Summary

Sheet: demo-blitter

File: demo-blitter.sch

Sheet: Demo GSTMCU

File: demo-gstmcu.sch

Sheet: Demo GSTMCU Mono-unit

File: demo-gstmcu-mono.sch

Sporny

Sheet: /

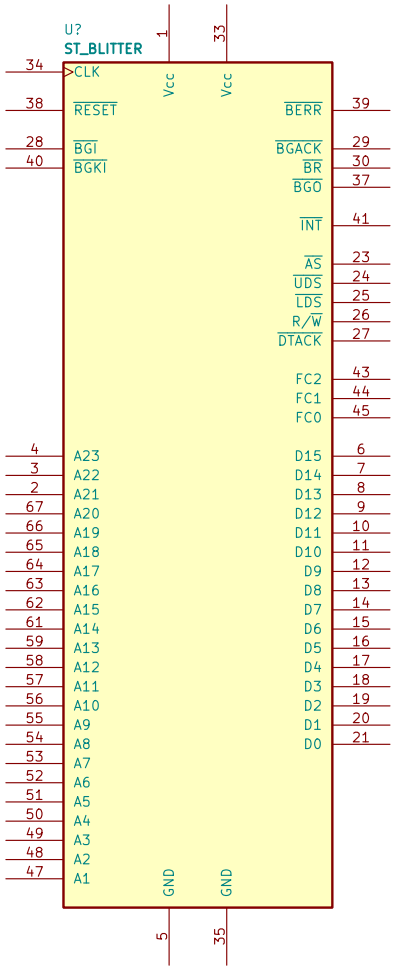
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Title: Exp

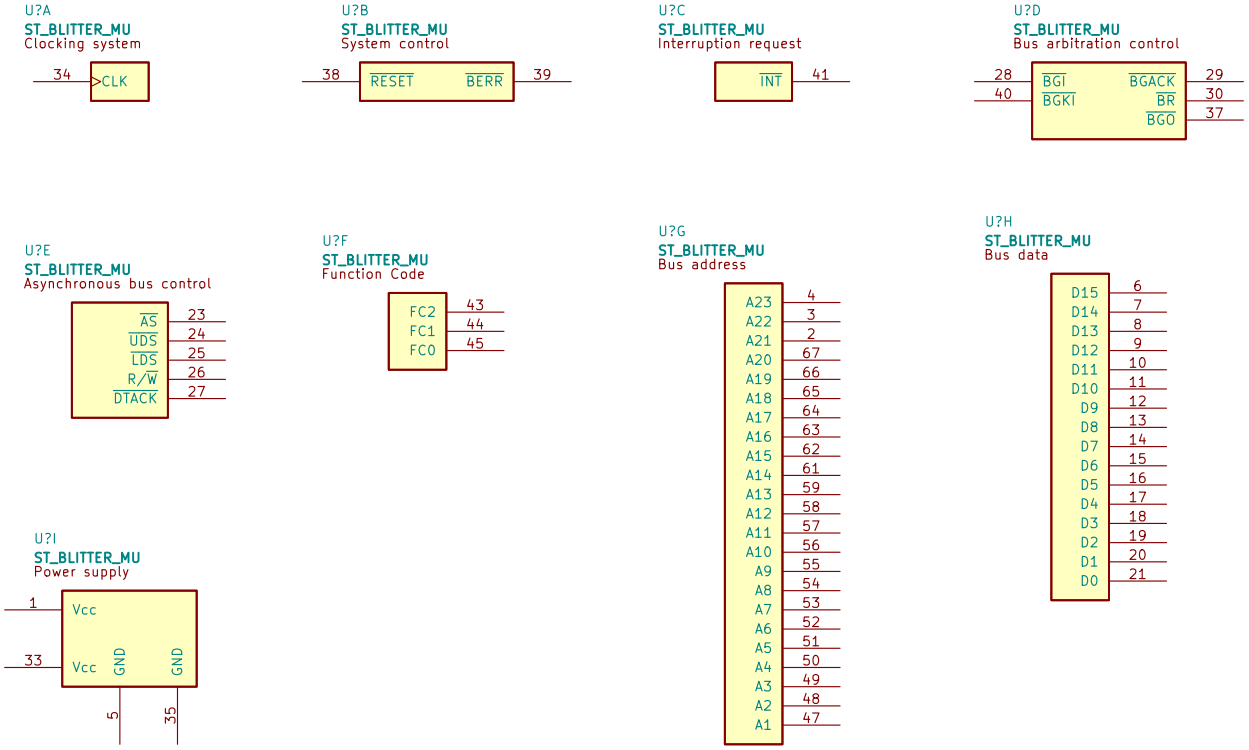
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Blitter demonstration

Single unit symbol



Multi-units symbol



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Demonstration of GSTMCU multi unit (single unit is tooo large)

U?A
STE_GSTMCU_MU
Clocking system
2 CLK16
CLK8 3
CLK0.5 6
CLK4 4
CLK2 5

U?B
STE_GSTMCU_MU
System control signals
66 RESET
BERR 23

U?C
STE_GSTMCU_MU
Bus arbitration control
28 BGI
BGACK 26
BGO 27
BR 29

U?D
STE_GSTMCU_MU
Asynchronous bus control
67 AS
68 UDS
69 LDS
70 R/W
DTACK 71

U?E
STE_GSTMCU_MU
Synchronous Bus control
24 VMA
VPA 25

U?F
STE_GSTMCU_MU
GLUE to MMU signals
DMA 132
RAM 133
DEV 134

U?G
STE_GSTMCU_MU
Drives interrupt signals
15 HDINT
16 FDINT
DISKINT 17

U?H
STE_GSTMCU_MU
MFP Interruption control
93 MFPINT
IACK 83
MFPCS 92

U?I
STE_GSTMCU_MU
Interrupt Priority Level selection
IPL0 33
IPL1 34
IPL2 35

U?J
STE_GSTMCU_MU
Function Code
38 FC2
39 FC1
40 FC0

U?K
STE_GSTMCU_MU
ROM area selection
ROM0 7
ROM1 8
ROM2 9
ROM3 10
ROM4 11
ROM5 12
ROM6 13

U?L
STE_GSTMCU_MU
RAM access control
WE 121
CAS1L 122
CAS1H 123
RAS1 124
CAS0L 125
CAS0H 126
RAS0 127

U?M
STE_GSTMCU_MU
Multiplexed ADDress bus (RAM)
MAD9 119
MAD8 118
MAD7 117
MAD6 116
MAD5 115
MAD4 114
MAD3 113
MAD2 112
MAD1 111
MAD0 110

U?N
STE_GSTMCU_MU
RAM access control for the Shifter
WDAT 129
RDAT 130
LATCH 131

U?O
STE_GSTMCU_MU
Video synchronisation
DCYC 138
CMPCS 139
BLANK 140
DE 141
VSYNC 142
HSYNC 143

U?P
STE_GSTMCU_MU
DMA Sound control
107 SREQ
SINT 105
SLOAD 106

U?Q
STE_GSTMCU_MU
Blitter control
60 BINT

U?R
STE_GSTMCU_MU
DMA chip control
135 RDY
FCS 136

U?S
STE_GSTMCU_MU
ACIA control
6850 49

U?T
STE_GSTMCU_MU
Programmable Sound Generator control
SNDCS 18
SNDIR 19

U?U
STE_GSTMCU_MU
Real Time Clock control
RTCWR 20
RTCRD 21
RTCCS 22

U?V
STE_GSTMCU_MU
Extended joysticks and paddles ports
94 PAD0X
95 PAD0Y
96 PAD1X
97 PAD1Y
98 PADRST
137 PEN
JOYRH 99
JOYRL 100
JOYWE 101
JOYWL 102
BUTTON 103

U?W
STE_GSTMCU_MU
External interrupt
30 EINT3
31 EINT5
32 EINT7

U?X
STE_GSTMCU_MU
Test
74 TEST

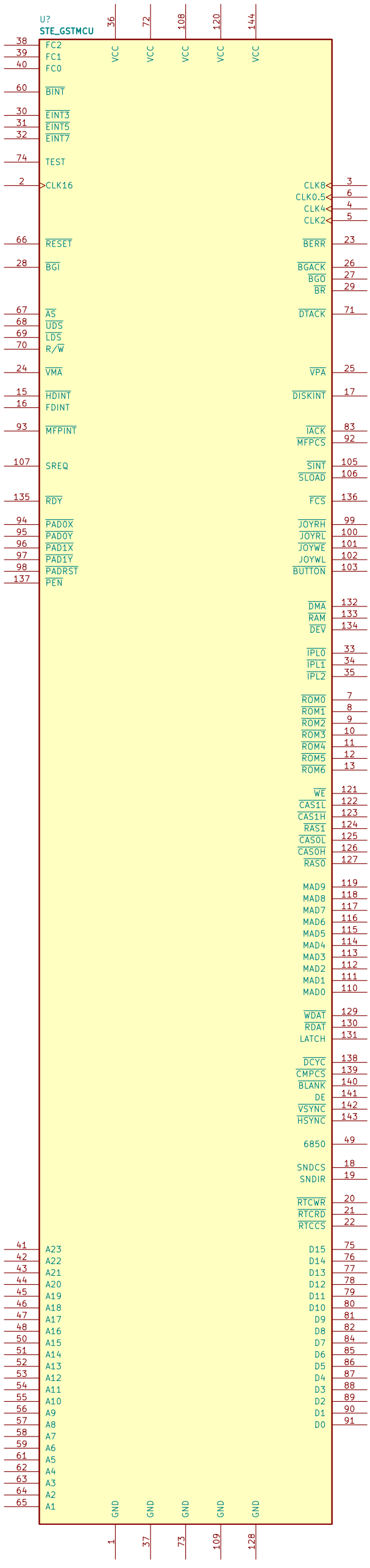
U?Y
STE_GSTMCU_MU
CPU bus address
A23 41
A22 42
A21 43
A20 44
A19 45
A18 46
A17 47
A16 48
A15 50
A14 51
A13 52
A12 53
A11 54
A10 55
A9 56
A8 57
A7 58
A6 59
A5 61
A4 62
A3 63
A2 64
A1 65

U?Z
STE_GSTMCU_MU
CPU bus data
D15 75
D14 76
D13 77
D12 78
D11 79
D10 80
D9 81
D8 82
D7 84
D6 85
D5 86
D4 87
D3 88
D2 89
D1 90
D0 91

U?AA
STE_GSTMCU_MU
Power supply
36 VCC
72 VCC
108 VCC
120 VCC
144 VCC
GND 1
GND 37
GND 73
GND 109
GND 128

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Demonstration of single unit GSTMCU – require A3 sheet size !



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