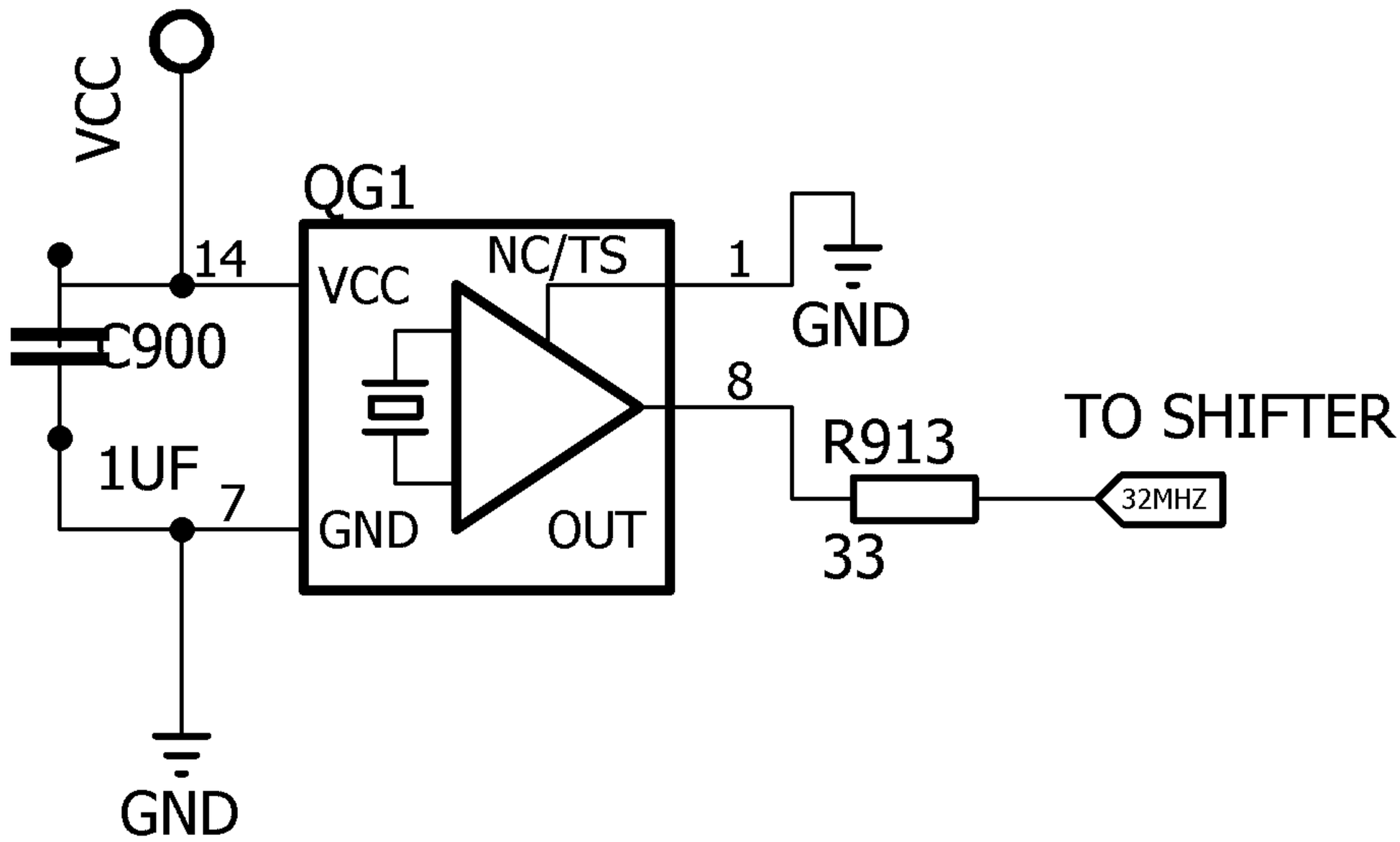
REV H5A (Phoenix) 2020-06-05 exxos

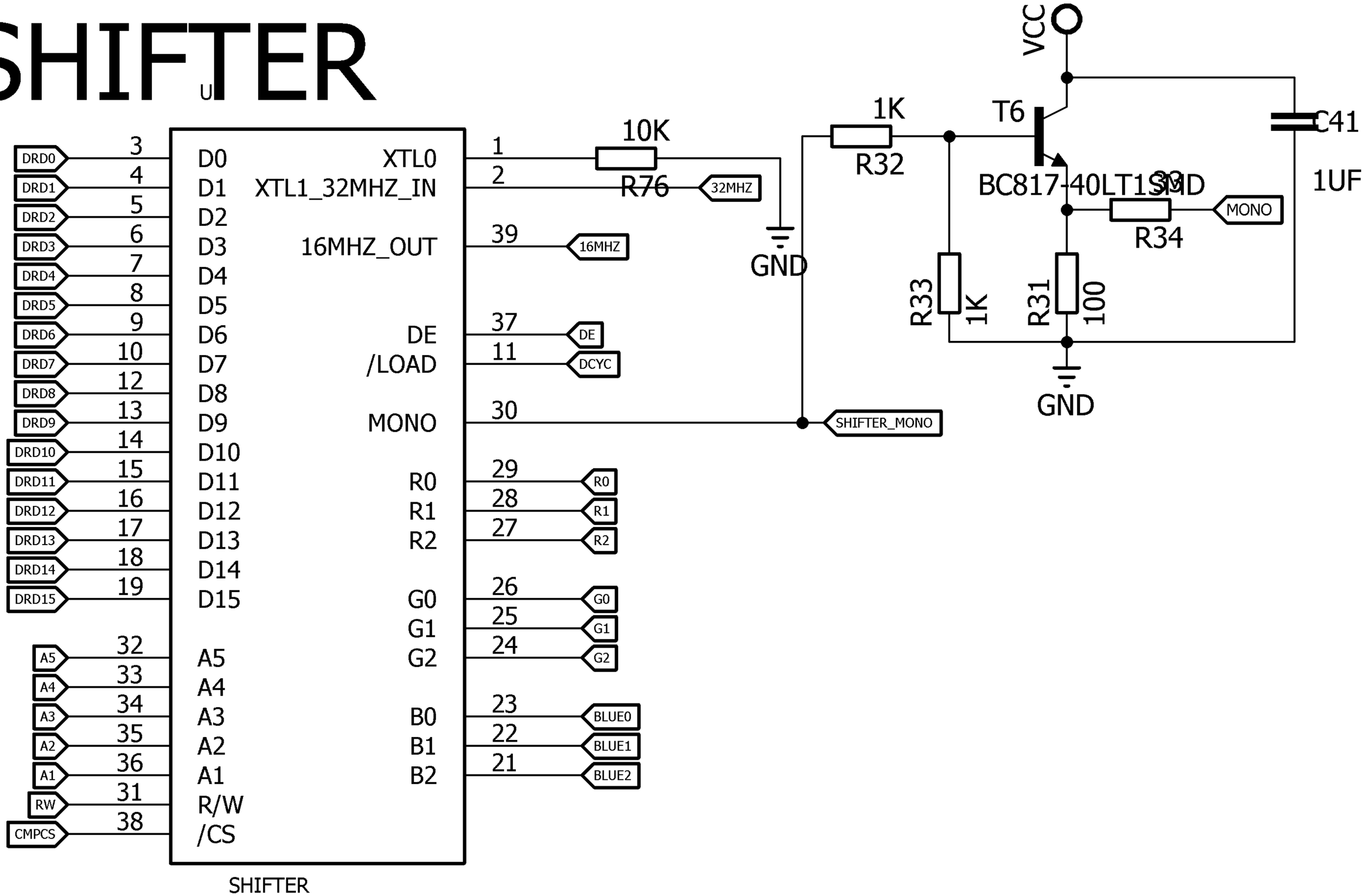
LOGOS

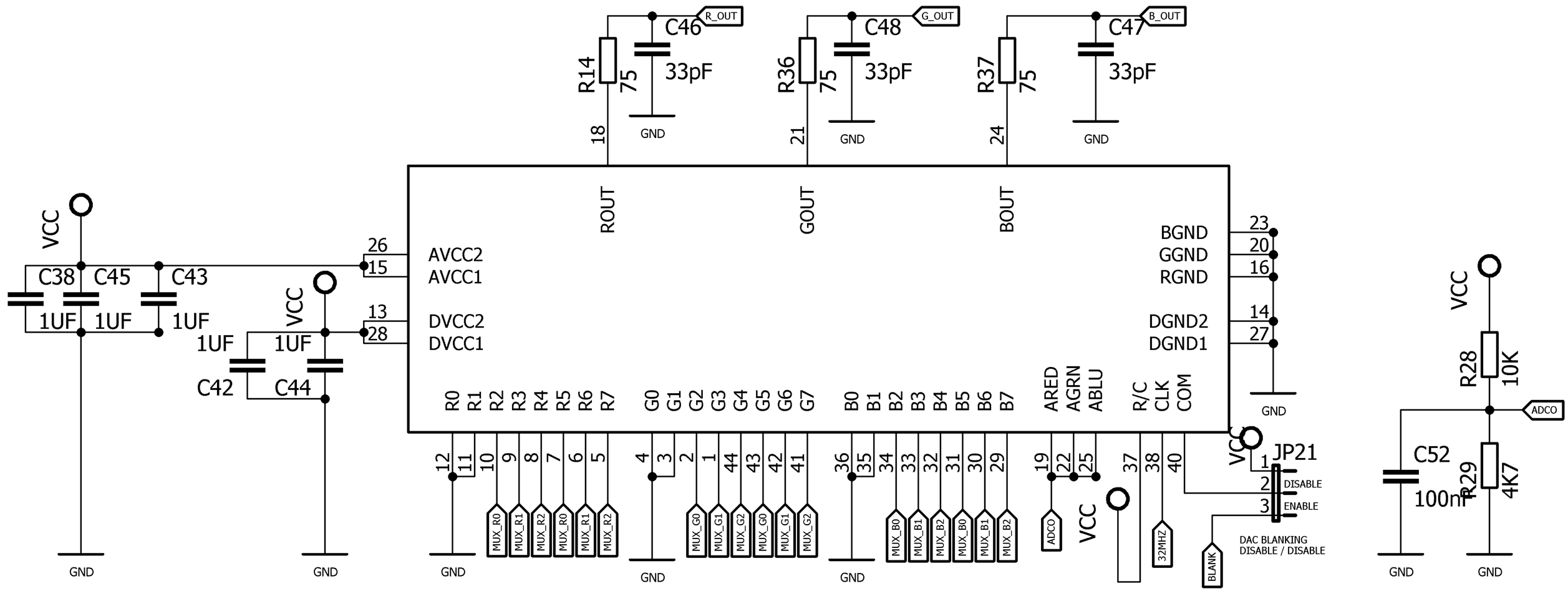
PHOENIX

32MHZ OSC

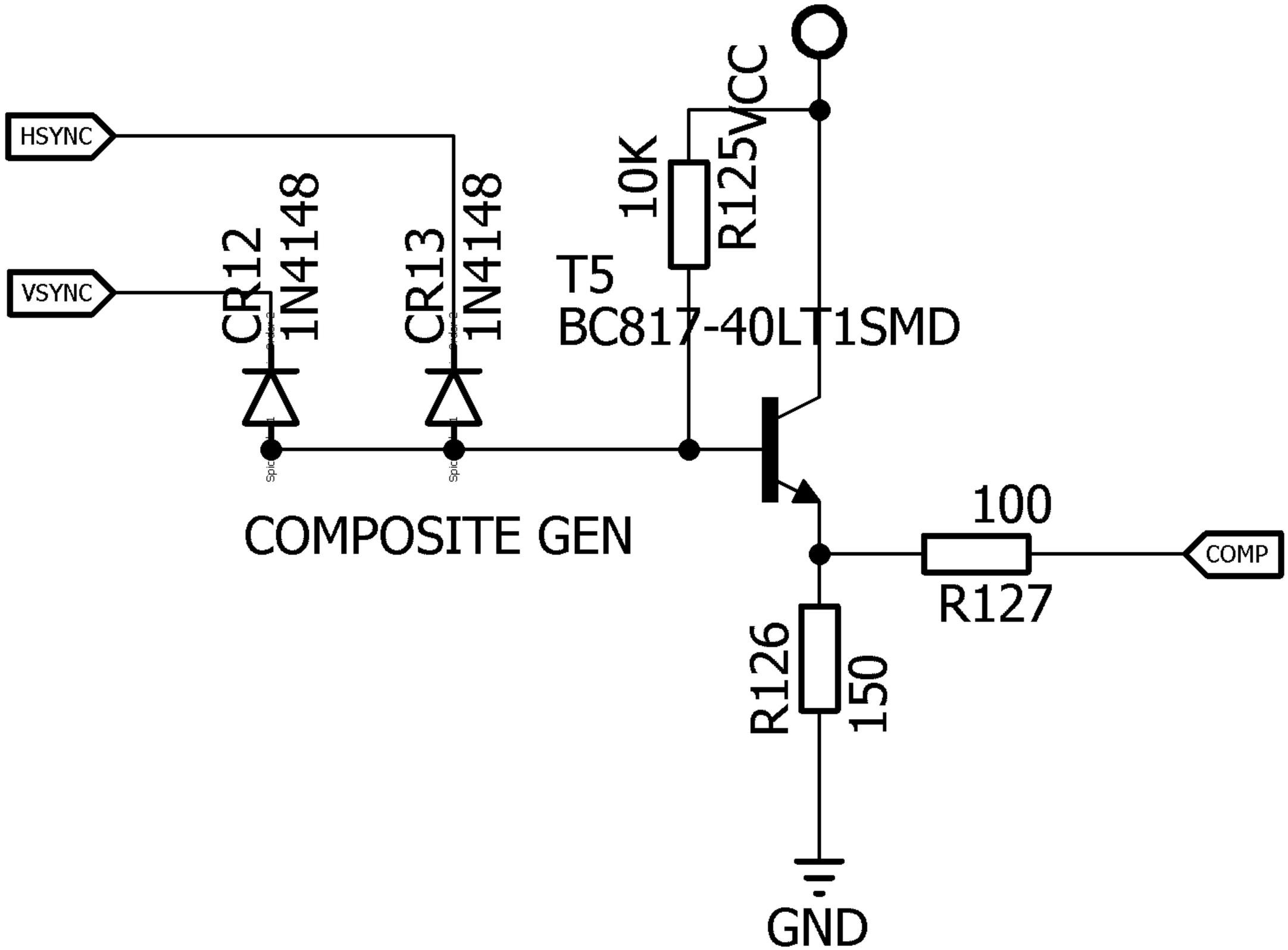

VCC
QG1
14
VCC
NC/TS
1
GND
C900
8
TO SHIFTER
R913
1UF
7
GND
OUT
32MHZ
33
GND

SHIFTER


U
DRD0
DRD1
DRD2
DRD3
DRD4
DRD5
DRD6
DRD7
DRD8
DRD9
DRD10
DRD11
DRD12
DRD13
DRD14
DRD15
A5
A4
A3
A2
A1
RW
CMPCS
3 D0
4 D1
5 D2
6 D3
7 D4
8 D5
9 D6
10 D7
12 D8
13 D9
14 D10
15 D11
16 D12
17 D13
18 D14
19 D15
32 A5
33 A4
34 A3
35 A2
36 A1
31 R/W
38 /CS
XTL0
XTL1_32MHZ_IN
16MHZ_OUT
DE
/LOAD
MONO
R0
R1
R2
G0
G1
G2
B0
B1
B2
1
2
39
37
11
30
29
28
27
26
25
24
23
22
21
10K
R76
32MHZ
16MHZ
DE
DCYC
GND
1K
R32
SHIFTER_MONO
VCC
T6
BC817-40LT1SMD
C41
1UF
R33
1K
R31
100
R34
MONO
GND
R0
R1
R2
G0
G1
G2
BLUE0
BLUE1
BLUE2
SHIFTER

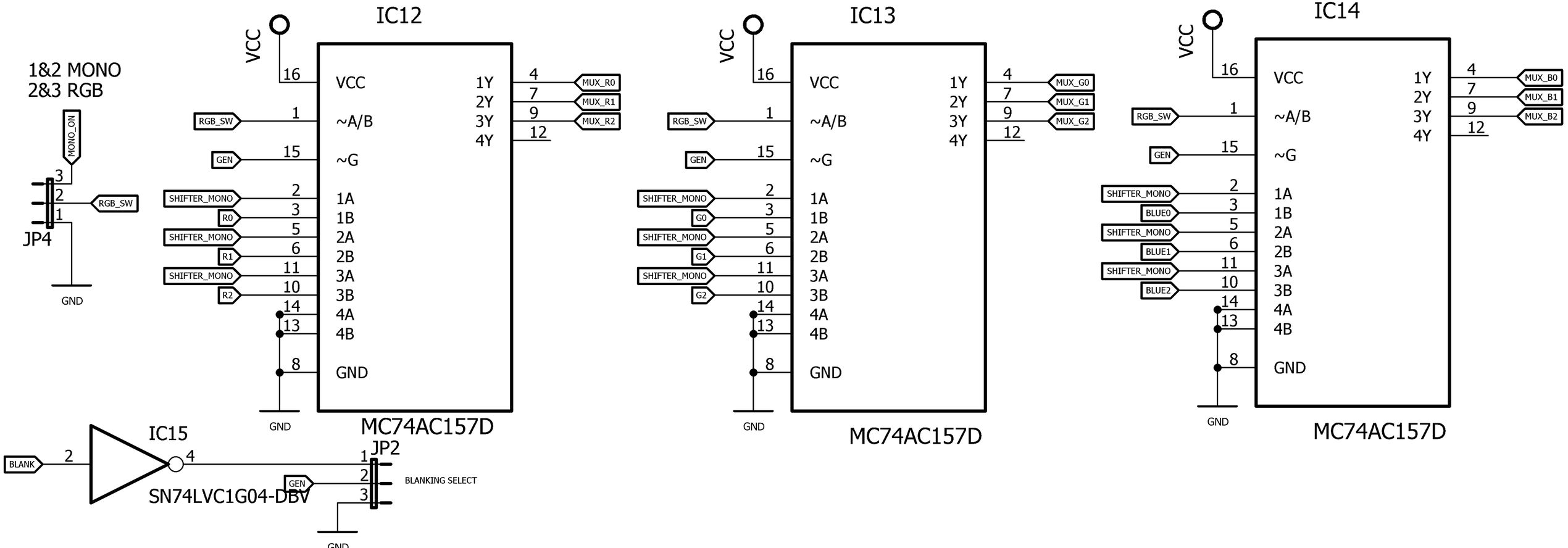

R_OUT
G_OUT
B_OUT
C46
C48
C47
R14
R36
R37
75
33pF
GND
18
21
24
ROUT
GOUT
BOUT
VCC
C38
C45
C43
1UF
26
15
13
28
AVCC2
AVCC1
DVCC2
DVCC1
C42
C44
BGND
GGND
RGND
DGND2
DGND1
23
20
16
14
27
R0 R1 R2 R3 R4 R5 R6 R7
G0 G1 G2 G3 G4 G5 G6 G7
B0 B1 B2 B3 B4 B5 B6 B7
ARED AGRN ABLU
R/C CLK COM
12 11 10 9 8 7 6 5
4 3 2 1 44 43 42 41
36 35 34 33 32 31 30 29
19 22 25
37 38 40
MUX_R0 MUX_R1 MUX_R2 MUX_R0 MUX_R1 MUX_R2
MUX_G0 MUX_G1 MUX_G2 MUX_G0 MUX_G1 MUX_G2
MUX_B0 MUX_B1 MUX_B2 MUX_B0 MUX_B1 MUX_B2
ADCO
32MHZ
BLANK
JP21
1
2
3
DISABLE
ENABLE
DAC BLANKING
DISABLE / DISABLE
R28
10K
R29
4K7
C52
100nF
ADCO

SYNC GEN

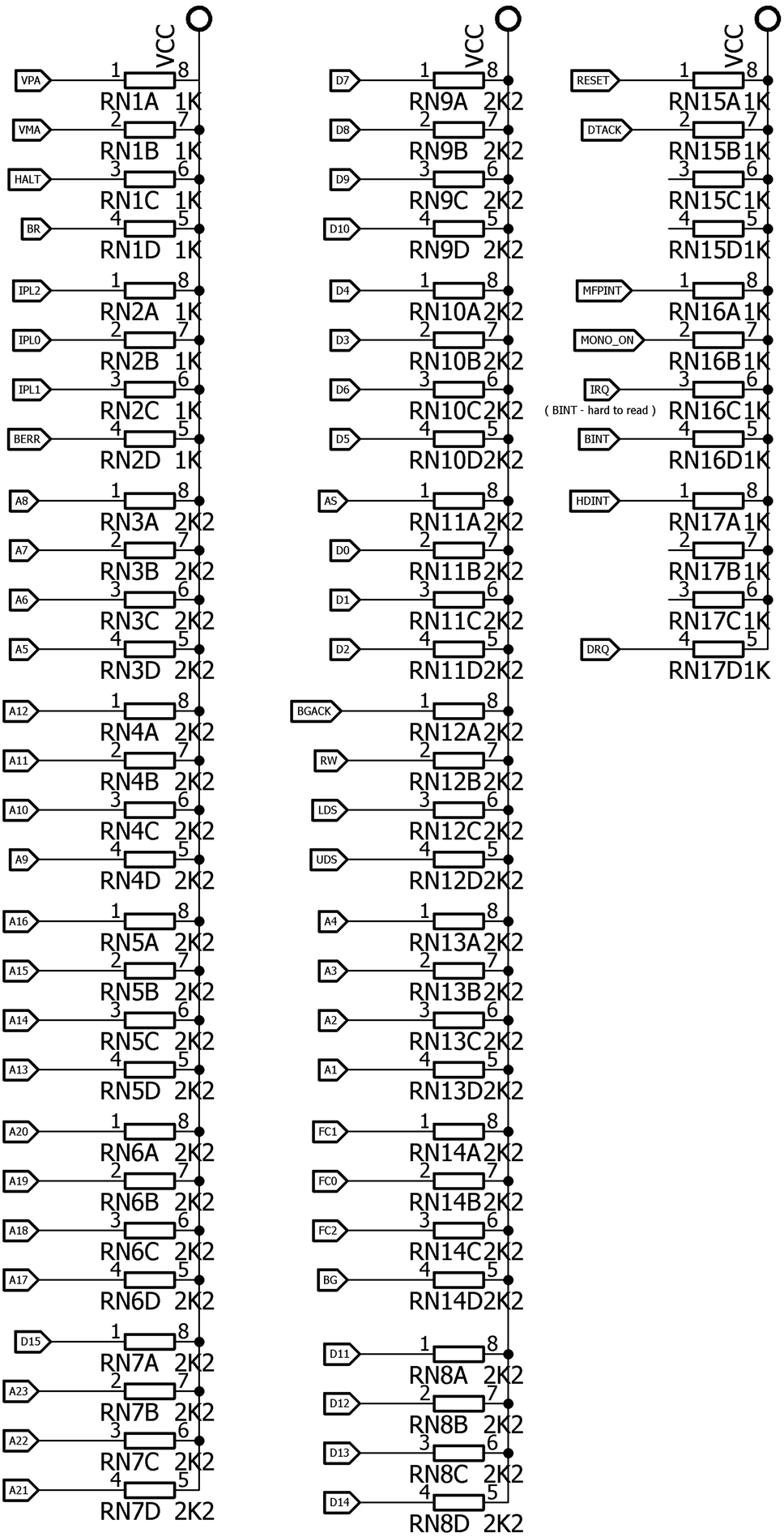

HSYNC
VSYNC
CR12
1N4148
CR13
1N4148
10K
R125
VCC
T5
BC817-40LT1SMD
COMPOSITE GEN
100
R127
COMP
R126
150
GND

RGB / MONO SWITCH

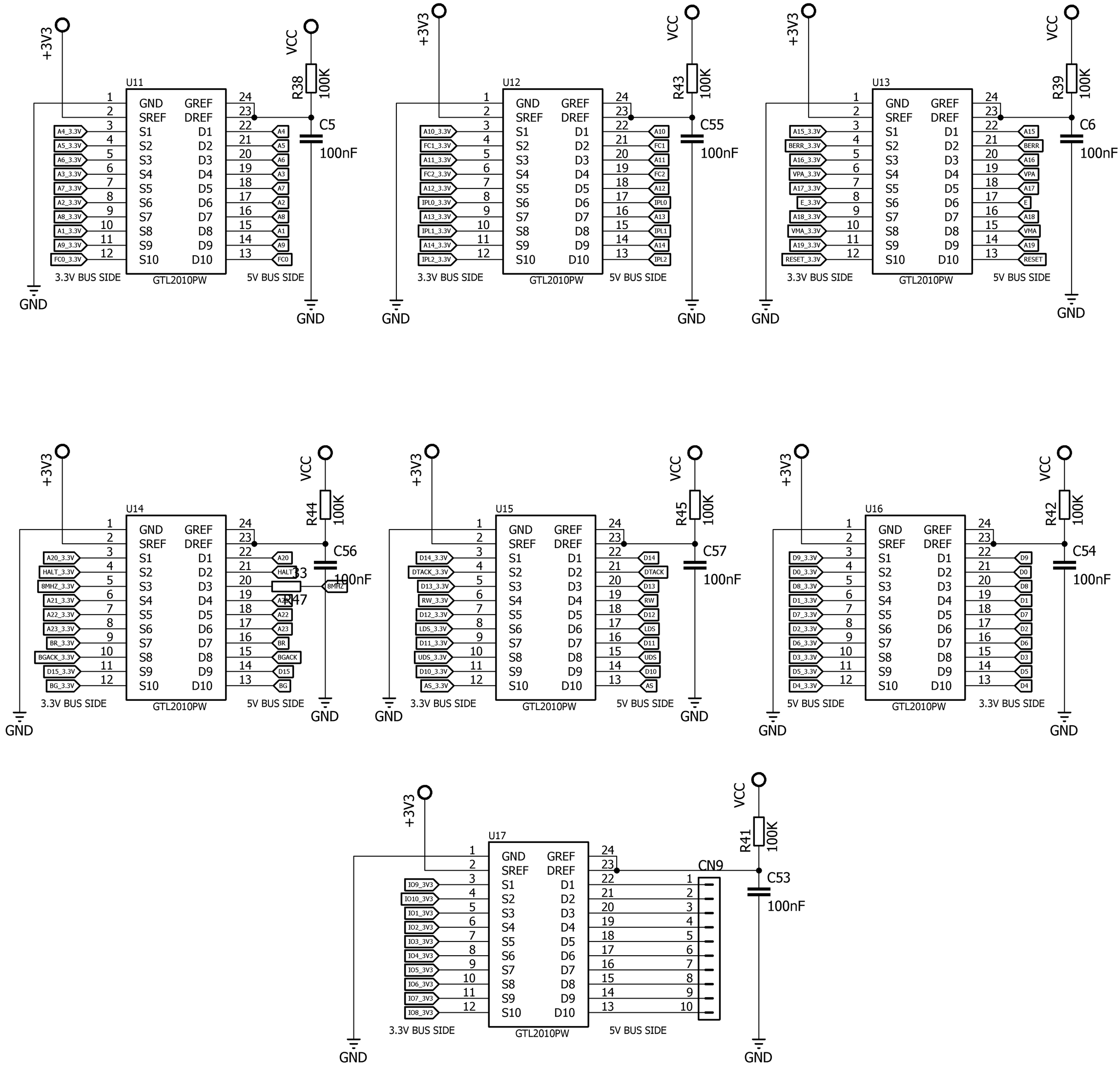
RGB/MONO LINES SWITCHED REV F



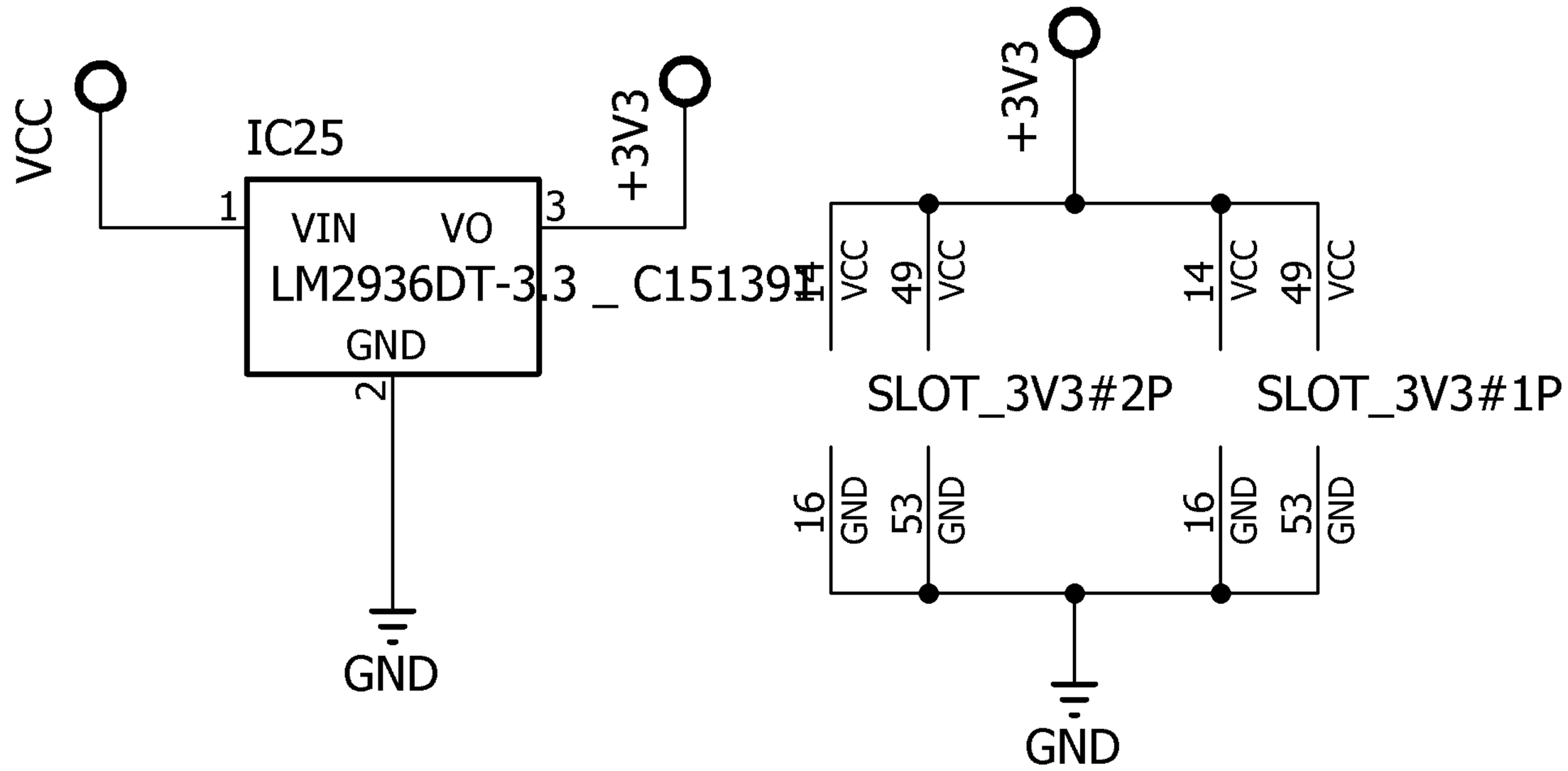
BUS PULL-UPS

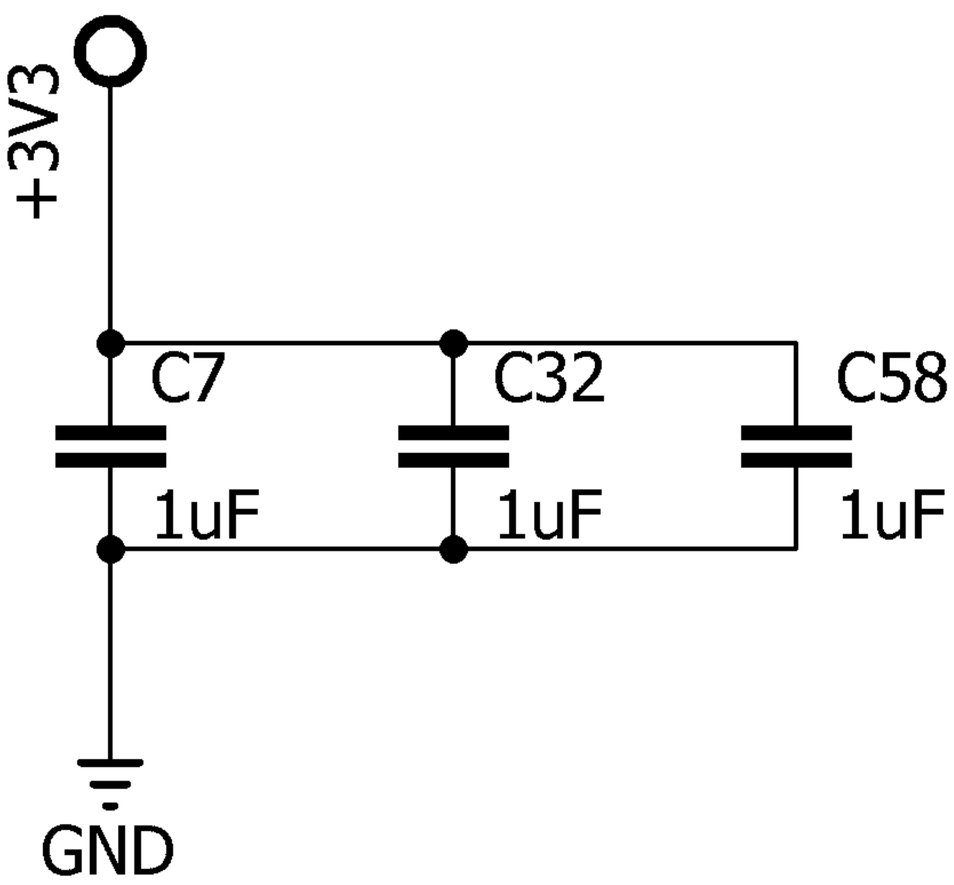

VCC
VPA
VMA
HALT
BR
RN1A 1K
RN1B 1K
RN1C 1K
RN1D 1K
IPL2
IPL0
IPL1
BERR
RN2A 1K
RN2B 1K
RN2C 1K
RN2D 1K
A8
A7
A6
A5
RN3A 2K2
RN3B 2K2
RN3C 2K2
RN3D 2K2
A12
A11
A10
A9
RN4A 2K2
RN4B 2K2
RN4C 2K2
RN4D 2K2
A16
A15
A14
A13
RN5A 2K2
RN5B 2K2
RN5C 2K2
RN5D 2K2
A20
A19
A18
A17
RN6A 2K2
RN6B 2K2
RN6C 2K2
RN6D 2K2
D15
A23
A22
A21
RN7A 2K2
RN7B 2K2
RN7C 2K2
RN7D 2K2
D7
D8
D9
D10
RN9A 2K2
RN9B 2K2
RN9C 2K2
RN9D 2K2
D4
D3
D6
D5
RN10A 2K2
RN10B 2K2
RN10C 2K2
RN10D 2K2
AS
D0
D1
D2
RN11A 2K2
RN11B 2K2
RN11C 2K2
RN11D 2K2
BGACK
RW
LDS
UDS
RN12A 2K2
RN12B 2K2
RN12C 2K2
RN12D 2K2
A4
A3
A2
A1
RN13A 2K2
RN13B 2K2
RN13C 2K2
RN13D 2K2
FC1
FC0
FC2
BG
RN14A 2K2
RN14B 2K2
RN14C 2K2
RN14D 2K2
D11
D12
D13
D14
RN8A 2K2
RN8B 2K2
RN8C 2K2
RN8D 2K2
RESET
DTACK
RN15A 1K
RN15B 1K
RN15C 1K
RN15D 1K
MFPINT
MONO_ON
IRQ
(BINT - hard to read)
BINT
RN16A 1K
RN16B 1K
RN16C 1K
RN16D 1K
HDINT
DRQ
RN17A 1K
RN17B 1K
RN17C 1K
RN17D 1K

3.3V BUS CONVERTORS

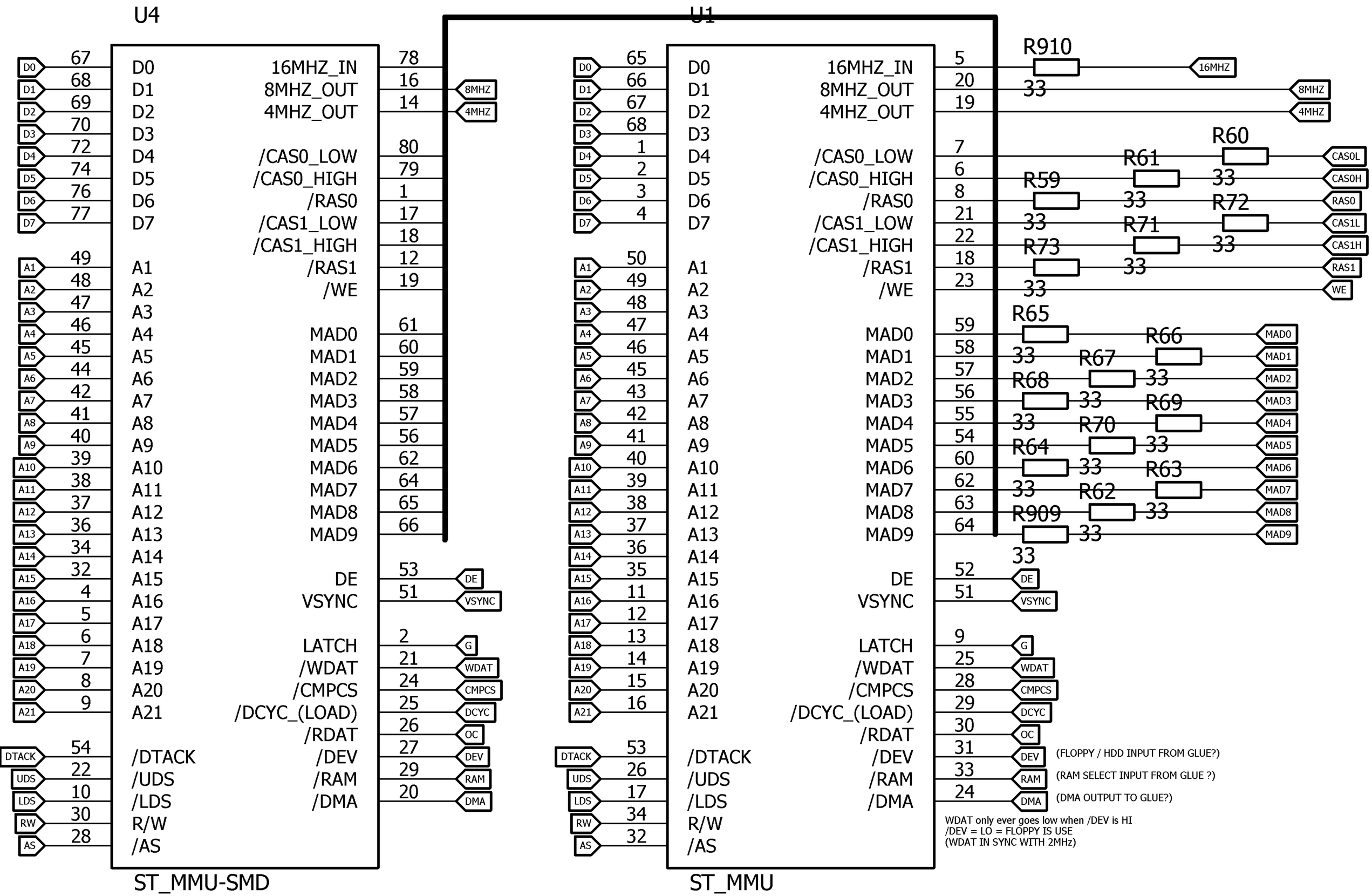


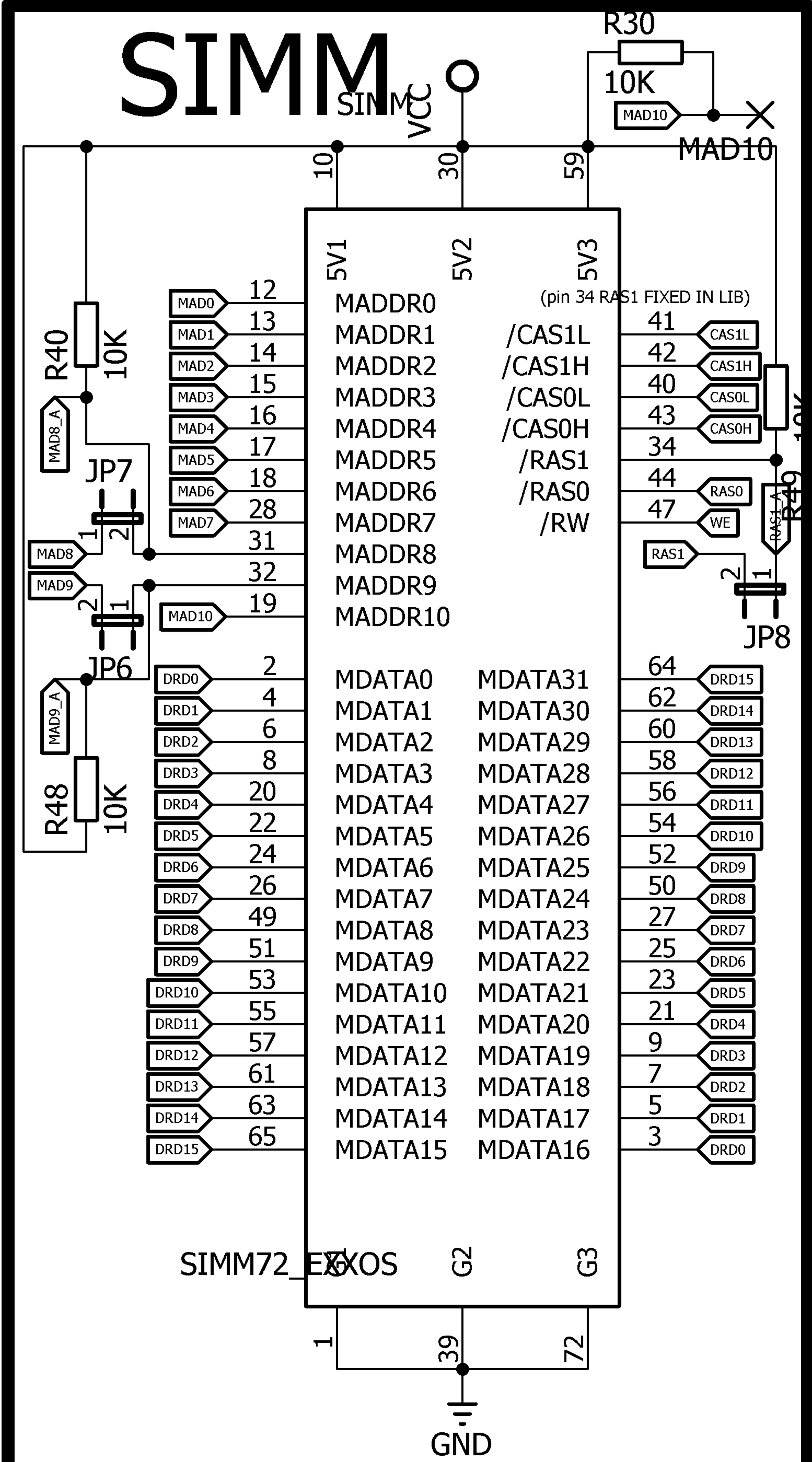
3.3V POWER


VCC
IC25
1
VIN
VO
3
LM2936DT-3.3 _ C15139
GND
2
+3V3
GND
+3V3
14
VCC
49
VCC
14
VCC
49
VCC
SLOT_3V3#2P
SLOT_3V3#1P
16
GND
53
GND
16
GND
53
GND
GND

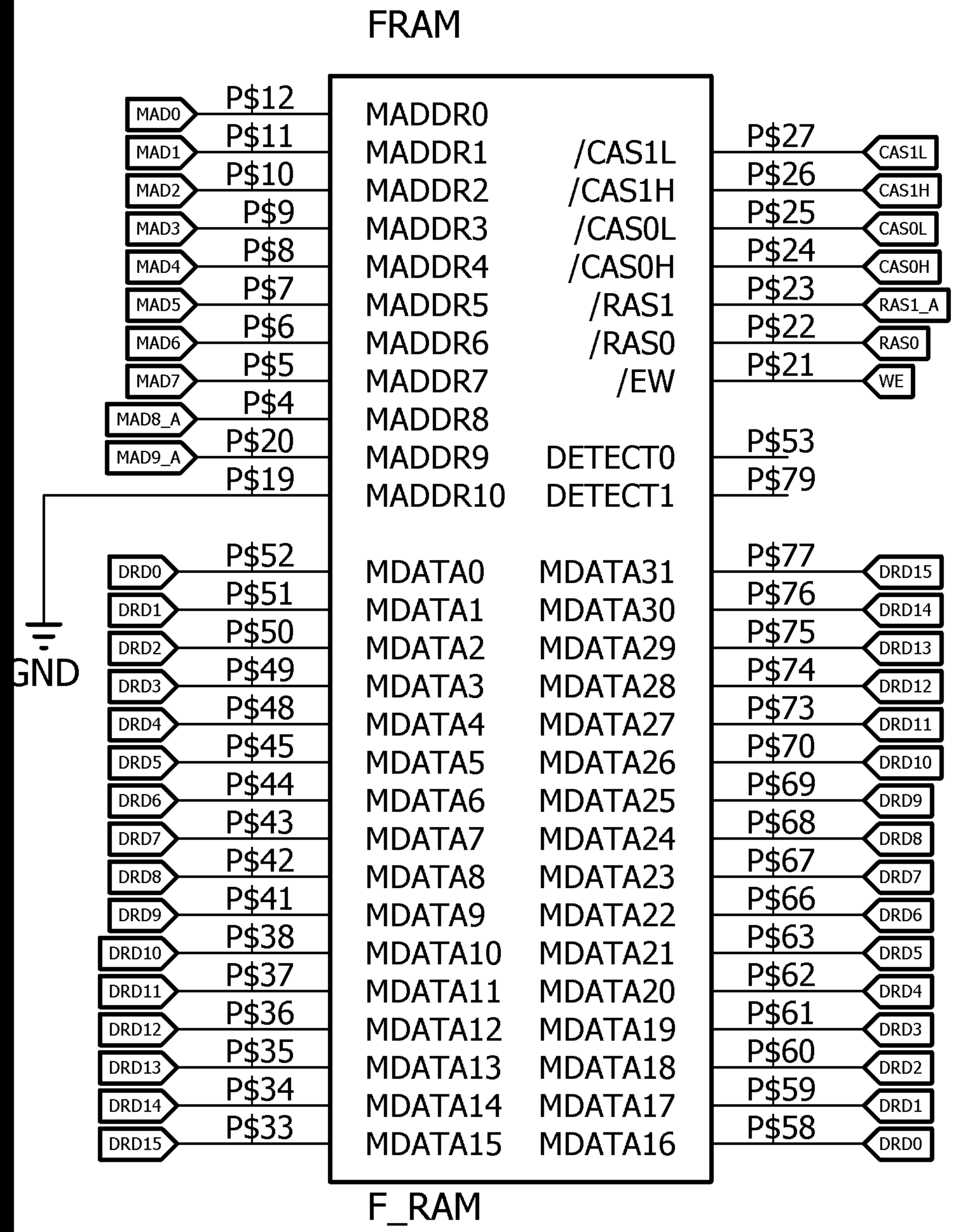

+3V3
C7
1uF
C32
1uF
C58
1uF
GND

MMU

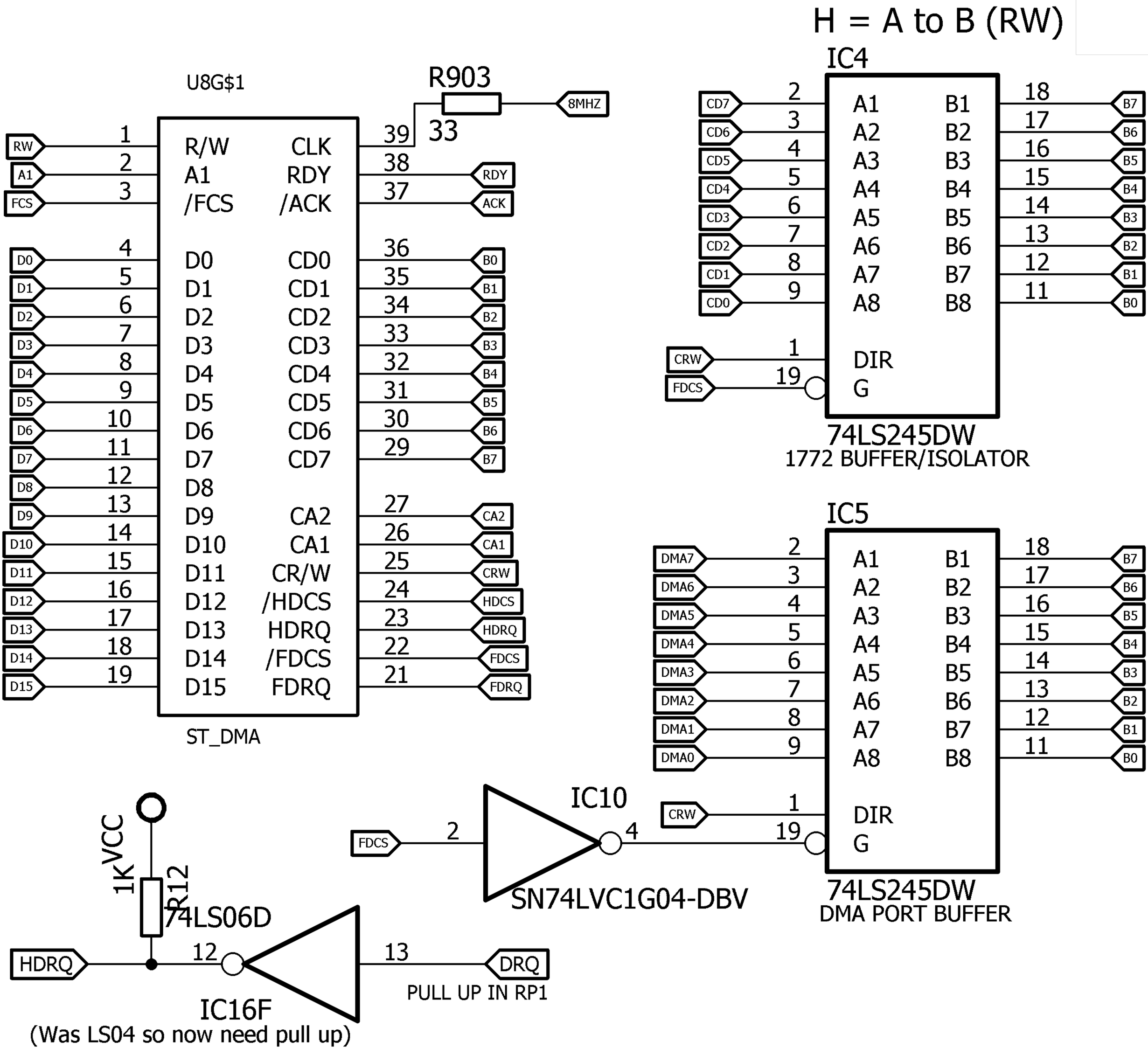

U4
D0 67 D0
D1 68 D1
D2 69 D2
D3 70 D3
D4 72 D4
D5 74 D5
D6 76 D6
D7 77 D7
A1 49 A1
A2 48 A2
A3 47 A3
A4 46 A4
A5 45 A5
A6 44 A6
A7 42 A7
A8 41 A8
A9 40 A9
A10 39 A10
A11 38 A11
A12 37 A12
A13 36 A13
A14 34 A14
A15 32 A15
A16 4 A16
A17 5 A17
A18 6 A18
A19 7 A19
A20 8 A20
A21 9 A21
DTACK 54 /DTACK
UDS 22 /UDS
LDS 10 /LDS
RW 30 R/W
AS 28 /AS
16MHZ_IN 78
8MHZ_OUT 16 8MHZ
4MHZ_OUT 14 4MHZ
/CAS0_LOW 80
/CAS0_HIGH 79
/RAS0 1
/CAS1_LOW 17
/CAS1_HIGH 18
/RAS1 12
/WE 19
MAD0 61
MAD1 60
MAD2 59
MAD3 58
MAD4 57
MAD5 56
MAD6 62
MAD7 64
MAD8 65
MAD9 66
DE 53 DE
VSYNC 51 VSYNC
LATCH 2 G
/WDAT 21 WDAT
/CMPCS 24 CMPCS
/DCYC_(LOAD) 25 DCYC
/RDAT 26 OC
/DEV 27 DEV
/RAM 29 RAM
/DMA 20 DMA
ST_MMU-SMD
U1
D0 65 D0
D1 66 D1
D2 67 D2
D3 68 D3
D4 1 D4
D5 2 D5
D6 3 D6
D7 4 D7
A1 50 A1
A2 49 A2
A3 48 A3
A4 47 A4
A5 46 A5
A6 45 A6
A7 43 A7
A8 42 A8
A9 41 A9
A10 40 A10
A11 39 A11
A12 38 A12
A13 37 A13
A14 36 A14
A15 35 A15
A16 11 A16
A17 12 A17
A18 13 A18
A19 14 A19
A20 15 A20
A21 16 A21
DTACK 53 /DTACK
UDS 26 /UDS
LDS 17 /LDS
RW 34 R/W
AS 32 /AS
16MHZ_IN 5
8MHZ_OUT 20
4MHZ_OUT 19
/CAS0_LOW 7
/CAS0_HIGH 6
/RAS0 8
/CAS1_LOW 21
/CAS1_HIGH 22
/RAS1 18
/WE 23
MAD0 59
MAD1 58
MAD2 57
MAD3 56
MAD4 55
MAD5 54
MAD6 60
MAD7 62
MAD8 63
MAD9 64
DE 52 DE
VSYNC 51 VSYNC
LATCH 9 G
/WDAT 25 WDAT
/CMPCS 28 CMPCS
/DCYC_(LOAD) 29 DCYC
/RDAT 30 OC
/DEV 31 DEV (FLOPPY / HDD INPUT FROM GLUE?)
/RAM 33 RAM (RAM SELECT INPUT FROM GLUE ?)
/DMA 24 DMA (DMA OUTPUT TO GLUE?)
WDAT only ever goes low when /DEV is HI
/DEV = LO = FLOPPY IS USE
(WDAT IN SYNC WITH 2MHz)
ST_MMU
R910 33 16MHZ
8MHZ
4MHZ
R60 33 CAS0L
R61 33 CAS0H
R59 33 RAS0
R72 33 CAS1L
R71 33 CAS1H
R73 33 RAS1
33 WE
R65 33 MAD0
R66 33 MAD1
R67 33 MAD2
R68 33 MAD3
R69 33 MAD4
R70 33 MAD5
R64 33 MAD6
R63 33 MAD7
R62 33 MAD8
R909 33 MAD9


SIMM
SIMM
VCC
R30
10K
MAD10
MAD10
10
30
59
5V1
5V2
5V3
(pin 34 RAS1 FIXED IN LIB)
R40
10K
MAD8_A
JP7
MAD8
MAD9
JP6
MAD9_A
R48
10K
MAD0
MAD1
MAD2
MAD3
MAD4
MAD5
MAD6
MAD7
MAD10
DRD0
DRD1
DRD2
DRD3
DRD4
DRD5
DRD6
DRD7
DRD8
DRD9
DRD10
DRD11
DRD12
DRD13
DRD14
DRD15
12
13
14
15
16
17
18
28
31
32
19
2
4
6
8
20
22
24
26
49
51
53
55
57
61
63
65
MADDR0
MADDR1
MADDR2
MADDR3
MADDR4
MADDR5
MADDR6
MADDR7
MADDR8
MADDR9
MADDR10
MDATA0
MDATA1
MDATA2
MDATA3
MDATA4
MDATA5
MDATA6
MDATA7
MDATA8
MDATA9
MDATA10
MDATA11
MDATA12
MDATA13
MDATA14
MDATA15
/CAS1L
/CAS1H
/CAS0L
/CAS0H
/RAS1
/RAS0
/RW
MDATA31
MDATA30
MDATA29
MDATA28
MDATA27
MDATA26
MDATA25
MDATA24
MDATA23
MDATA22
MDATA21
MDATA20
MDATA19
MDATA18
MDATA17
MDATA16
41
42
40
43
34
44
47
CAS1L
CAS1H
CAS0L
CAS0H
RAS0
WE
RAS1
RAS1_A
R49
10K
JP8
64
62
60
58
56
54
52
50
27
25
23
21
9
7
5
3
DRD15
DRD14
DRD13
DRD12
DRD11
DRD10
DRD9
DRD8
DRD7
DRD6
DRD5
DRD4
DRD3
DRD2
DRD1
DRD0
SIMM72_EXXOS
G2
G3
1
39
72
GND

DRAM_FALC

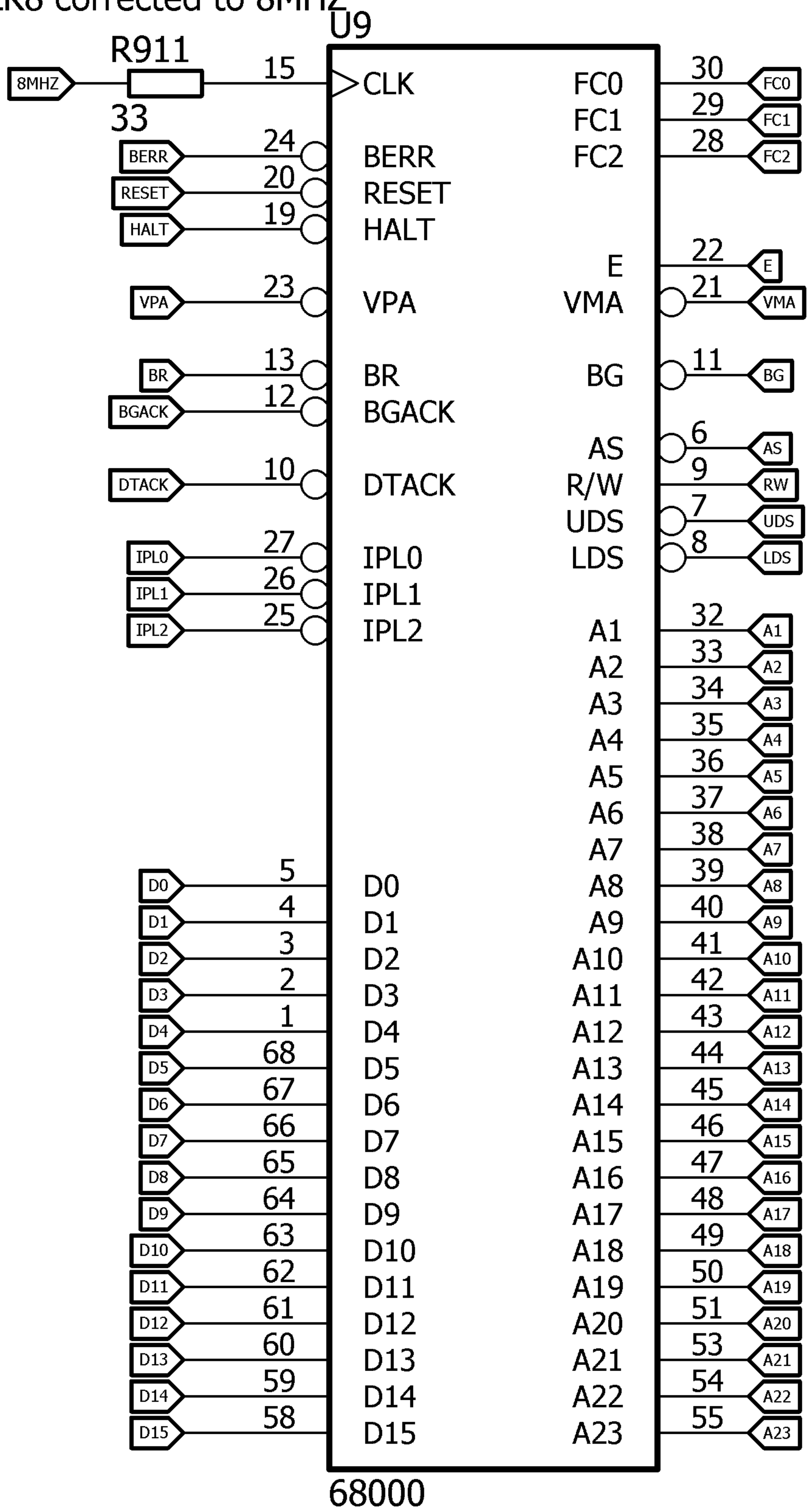

FRAM
MADDR0
MADDR1
MADDR2
MADDR3
MADDR4
MADDR5
MADDR6
MADDR7
MADDR8
MADDR9
MADDR10
/CAS1L
/CAS1H
/CAS0L
/CAS0H
/RAS1
/RAS0
/EW
DETECT0
DETECT1
MDATA0
MDATA1
MDATA2
MDATA3
MDATA4
MDATA5
MDATA6
MDATA7
MDATA8
MDATA9
MDATA10
MDATA11
MDATA12
MDATA13
MDATA14
MDATA15
MDATA31
MDATA30
MDATA29
MDATA28
MDATA27
MDATA26
MDATA25
MDATA24
MDATA23
MDATA22
MDATA21
MDATA20
MDATA19
MDATA18
MDATA17
MDATA16
MAD0 P$12
MAD1 P$11
MAD2 P$10
MAD3 P$9
MAD4 P$8
MAD5 P$7
MAD6 P$6
MAD7 P$5
MAD8_A P$4
MAD9_A P$20
P$19
GND
DRD0 P$52
DRD1 P$51
DRD2 P$50
DRD3 P$49
DRD4 P$48
DRD5 P$45
DRD6 P$44
DRD7 P$43
DRD8 P$42
DRD9 P$41
DRD10 P$38
DRD11 P$37
DRD12 P$36
DRD13 P$35
DRD14 P$34
DRD15 P$33
P$27 CAS1L
P$26 CAS1H
P$25 CAS0L
P$24 CAS0H
P$23 RAS1_A
P$22 RAS0
P$21 WE
P$53
P$79
P$77 DRD15
P$76 DRD14
P$75 DRD13
P$74 DRD12
P$73 DRD11
P$70 DRD10
P$69 DRD9
P$68 DRD8
P$67 DRD7
P$66 DRD6
P$63 DRD5
P$62 DRD4
P$61 DRD3
P$60 DRD2
P$59 DRD1
P$58 DRD0
F_RAM

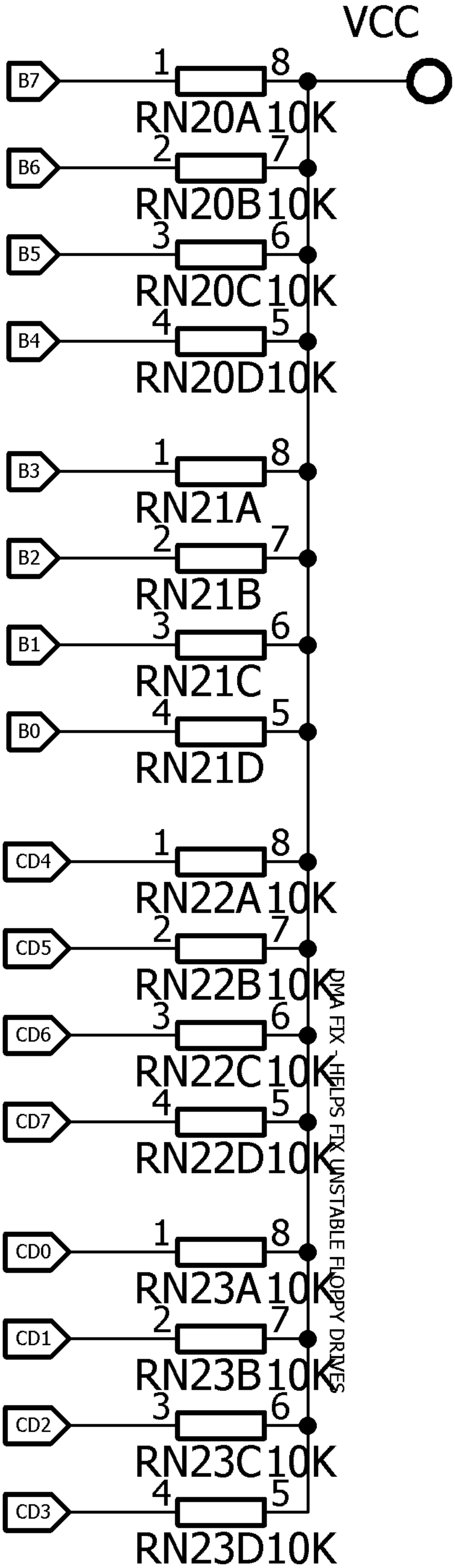
DMA & WD1772

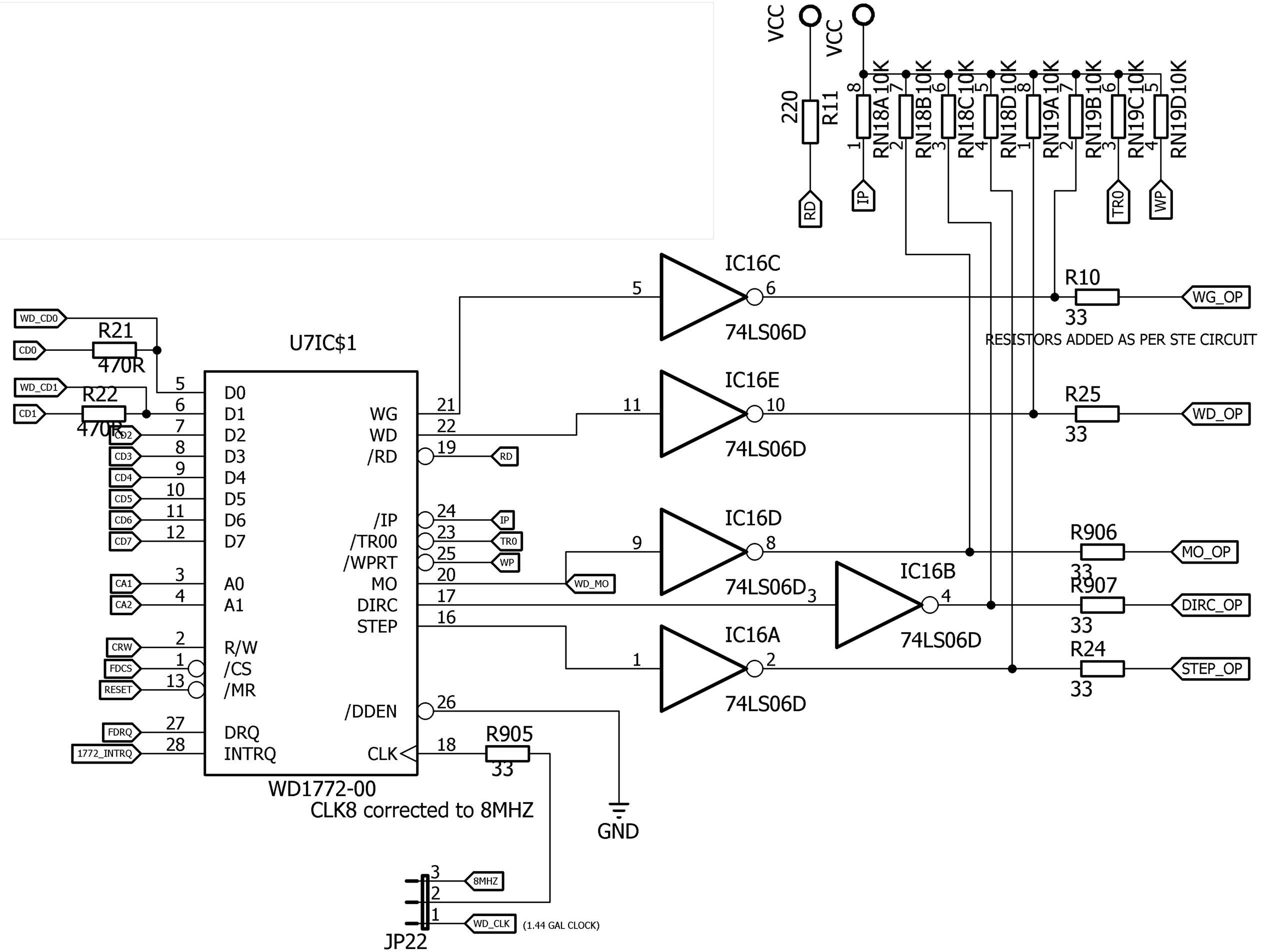

H = A to B (RW)
U8G$1
R903
33
8MHZ
RW
A1
FCS
R/W
A1
/FCS
CLK
RDY
/ACK
RDY
ACK
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
CD0
CD1
CD2
CD3
CD4
CD5
CD6
CD7
CA2
CA1
CR/W
/HDCS
HDRQ
/FDCS
FDRQ
B0
B1
B2
B3
B4
B5
B6
B7
CA2
CA1
CRW
HDCS
HDRQ
FDCS
FDRQ
ST_DMA
IC4
CD7
CD6
CD5
CD4
CD3
CD2
CD1
CD0
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
CRW
FDCS
DIR
G
74LS245DW
1772 BUFFER/ISOLATOR
IC5
DMA7
DMA6
DMA5
DMA4
DMA3
DMA2
DMA1
DMA0
CRW
DIR
G
74LS245DW
DMA PORT BUFFER
IC10
FDCS
SN74LVC1G04-DBV
VCC
1K
R12
74LS06D
HDRQ
IC16F
(Was LS04 so now need pull up)
DRQ
PULL UP IN RP1

68000 CPU

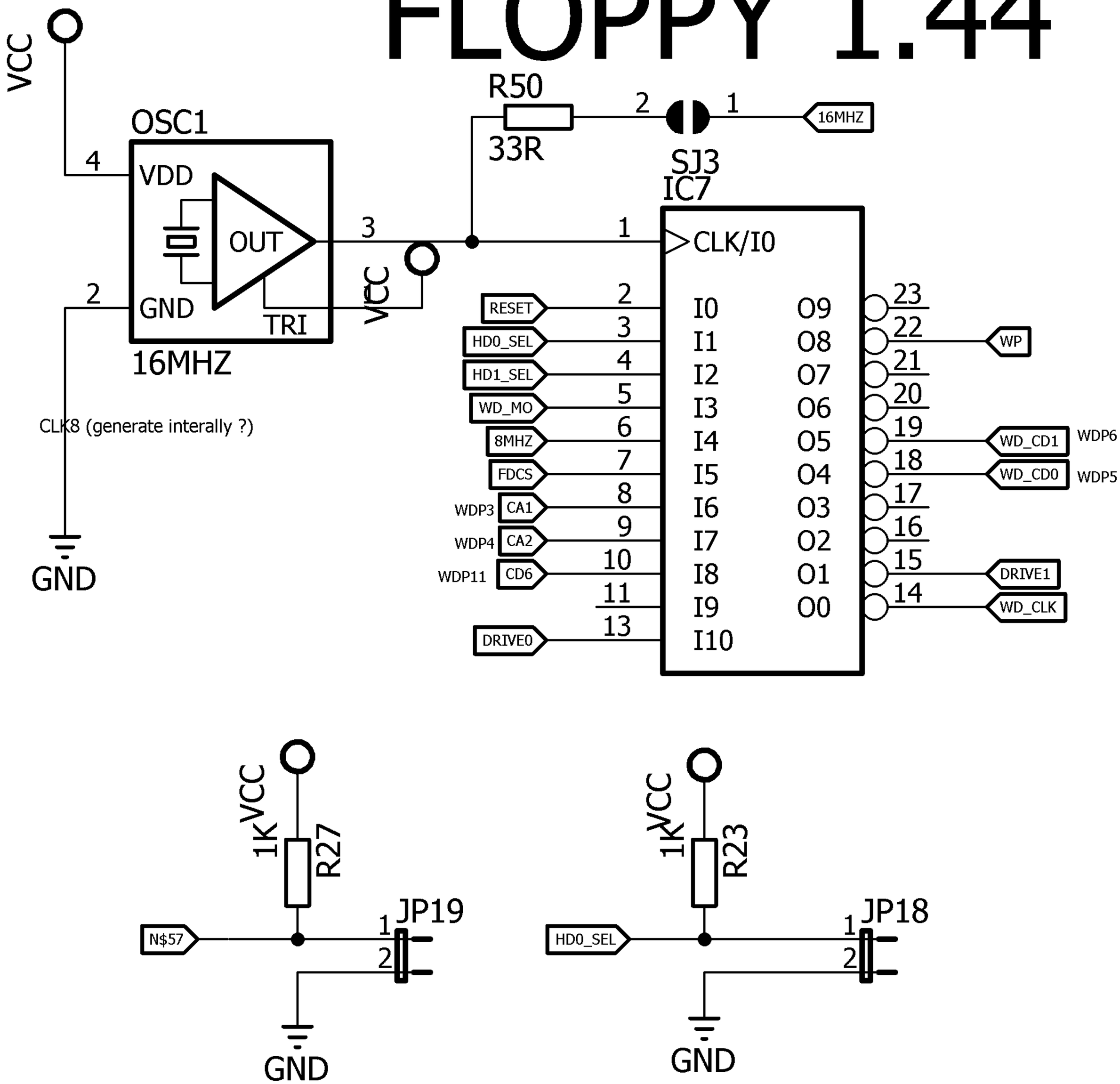
CLK8 corrected to 8MHZ



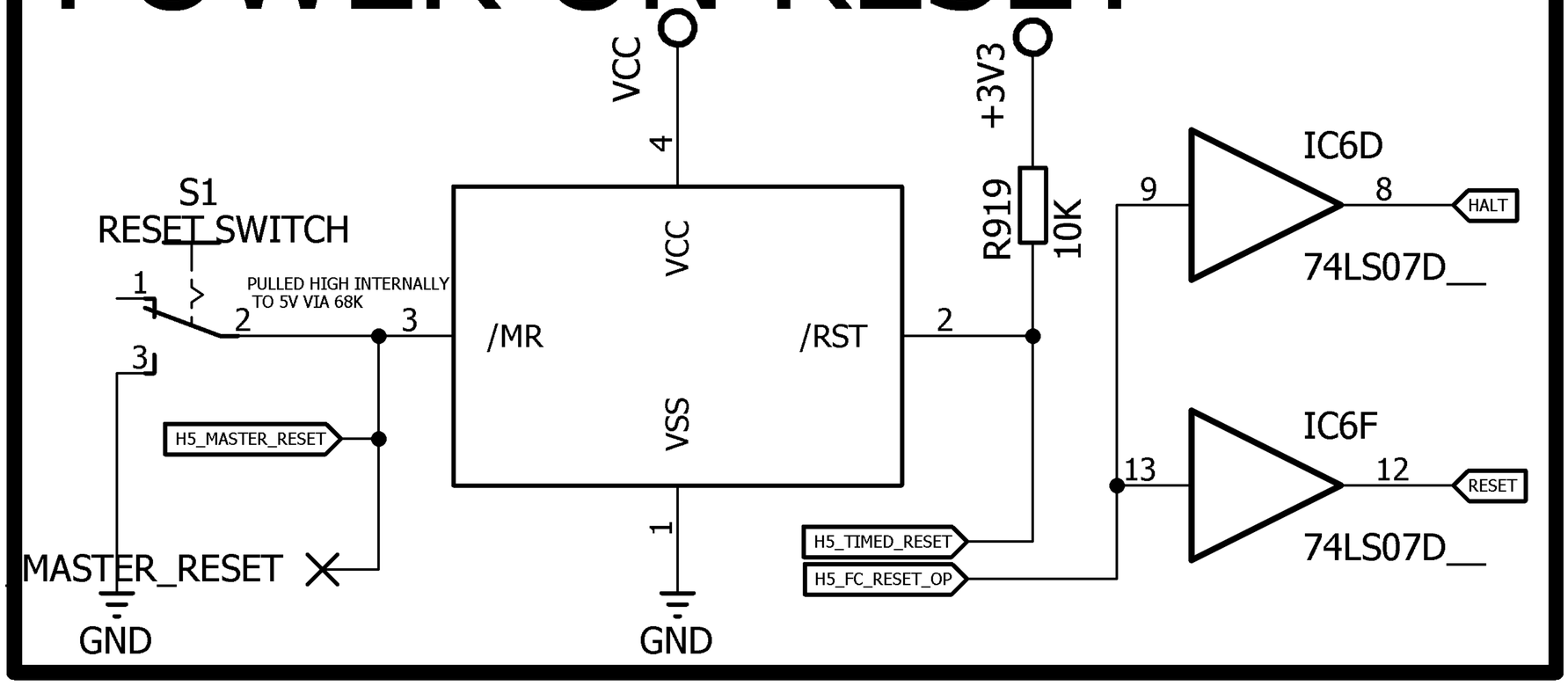

VCC
B7
B6
B5
B4
B3
B2
B1
B0
CD4
CD5
CD6
CD7
CD0
CD1
CD2
CD3
RN20A 10K
RN20B 10K
RN20C 10K
RN20D 10K
RN21A
RN21B
RN21C
RN21D
RN22A 10K
RN22B 10K
RN22C 10K
RN22D 10K
RN23A 10K
RN23B 10K
RN23C 10K
RN23D 10K
DMA FIX - HELPS FIX UNSTABLE FLOPPY DRIVES


VCC
VCC
220
R11
RN18A 10K
RN18B 10K
RN18C 10K
RN18D 10K
RN19A 10K
RN19B 10K
RN19C 10K
RN19D 10K
RD
IP
TR0
WP
IC16C
74LS06D
IC16E
74LS06D
IC16D
74LS06D
IC16B
74LS06D
IC16A
74LS06D
R10
33
WG_OP
RESISTORS ADDED AS PER STE CIRCUIT
R25
33
WD_OP
R906
33
MO_OP
R907
33
DIRC_OP
R24
33
STEP_OP
WD_CD0
CD0
R21
470R
WD_CD1
CD1
R22
470R
CD2
CD3
CD4
CD5
CD6
CD7
CA1
CA2
CRW
FDCS
RESET
FDRQ
1772_INTRQ
U7IC$1
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
R/W
/CS
/MR
DRQ
INTRQ
WG
WD
/RD
/IP
/TR00
/WPRT
MO
DIRC
STEP
/DDEN
CLK
WD_MO
R905
33
WD1772-00
CLK8 corrected to 8MHZ
GND
8MHZ
WD_CLK
(1.44 GAL CLOCK)
JP22

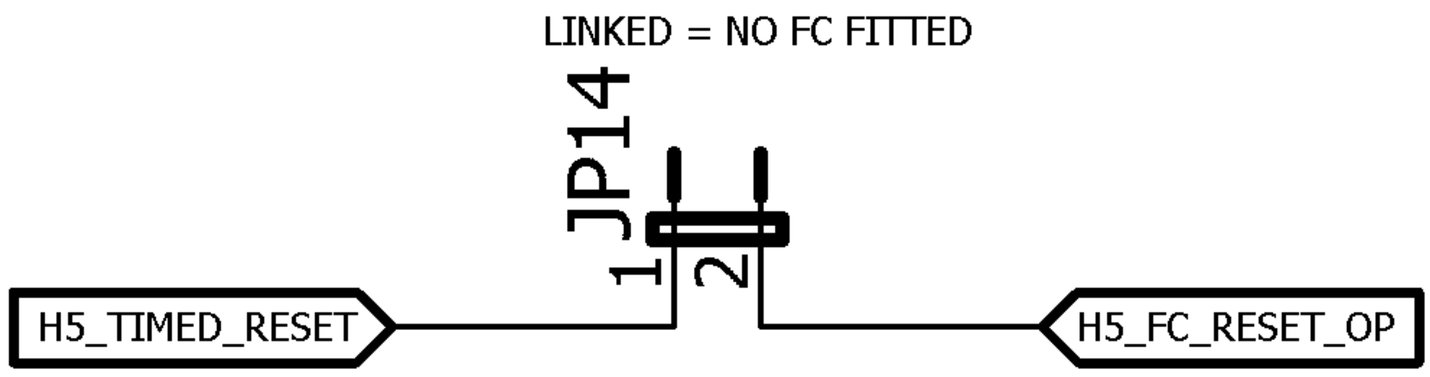
FLOPPY 1.44

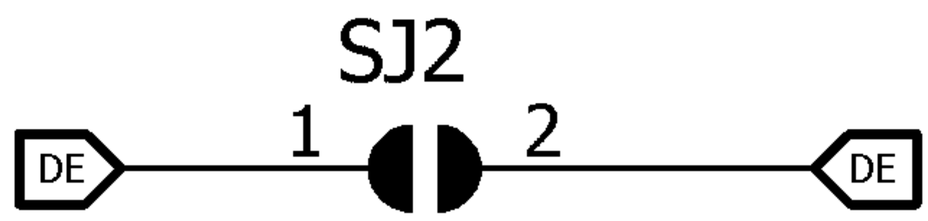

VCC
OSC1
VDD
OUT
GND
TRI
16MHZ
CLK8 (generate interally ?)
GND
R50
33R
SJ3
16MHZ
IC7
CLK/I0
RESET
HD0_SEL
HD1_SEL
WD_MO
8MHZ
FDCS
WDP3 CA1
WDP4 CA2
WDP11 CD6
DRIVE0
I0
I1
I2
I3
I4
I5
I6
I7
I8
I9
I10
O9
O8
O7
O6
O5
O4
O3
O2
O1
O0
WP
WD_CD1
WDP6
WD_CD0
WDP5
DRIVE1
WD_CLK
VCC
1K
R27
N$57
JP19
GND
VCC
1K
R23
HD0_SEL
JP18
GND

POWER ON RESET

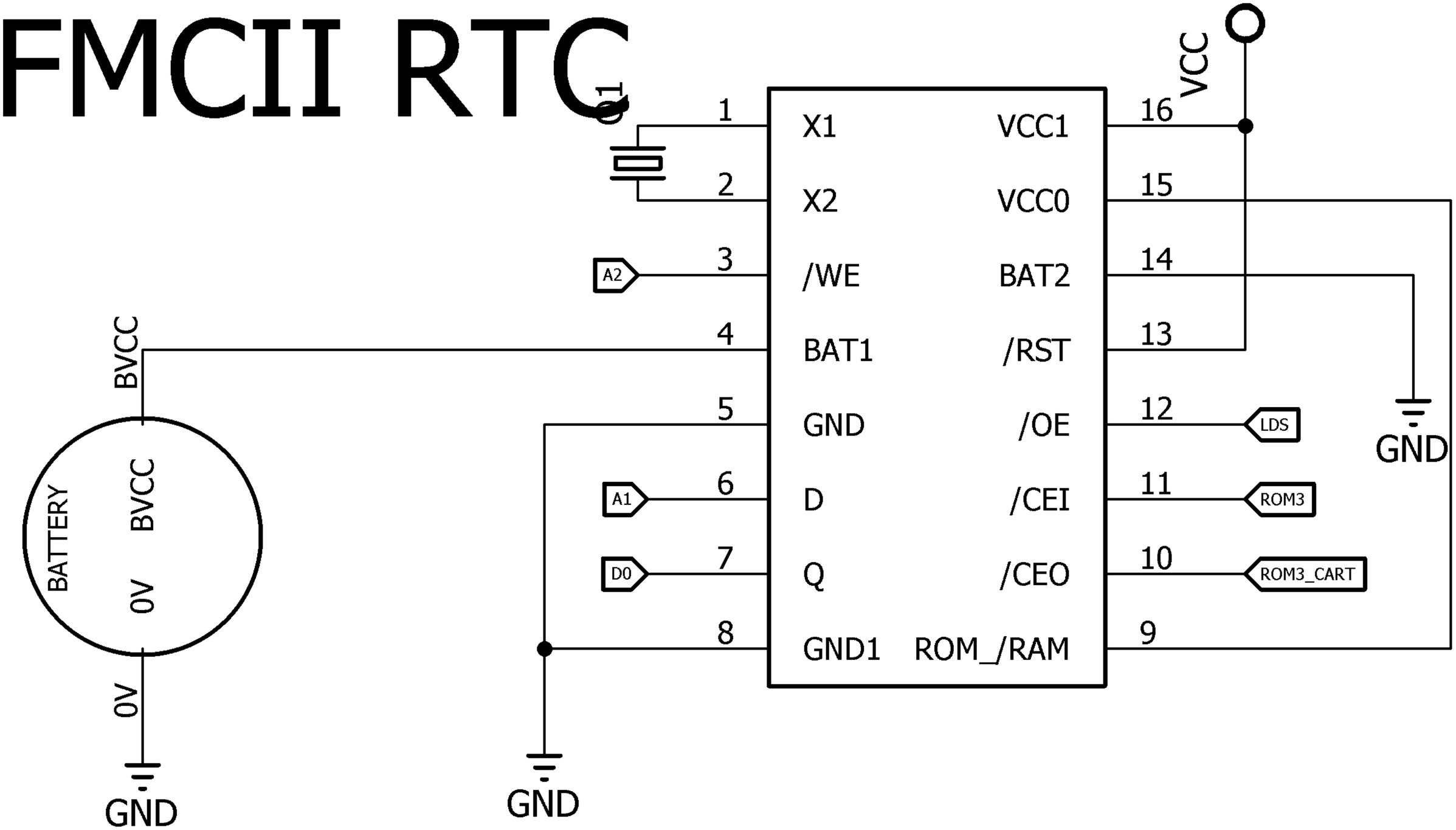


JUMPERS


LINKED = NO FC FITTED
JP14
1
2
H5_TIMED_RESET
H5_FC_RESET_OP


SJ2
1
2
DE
DE

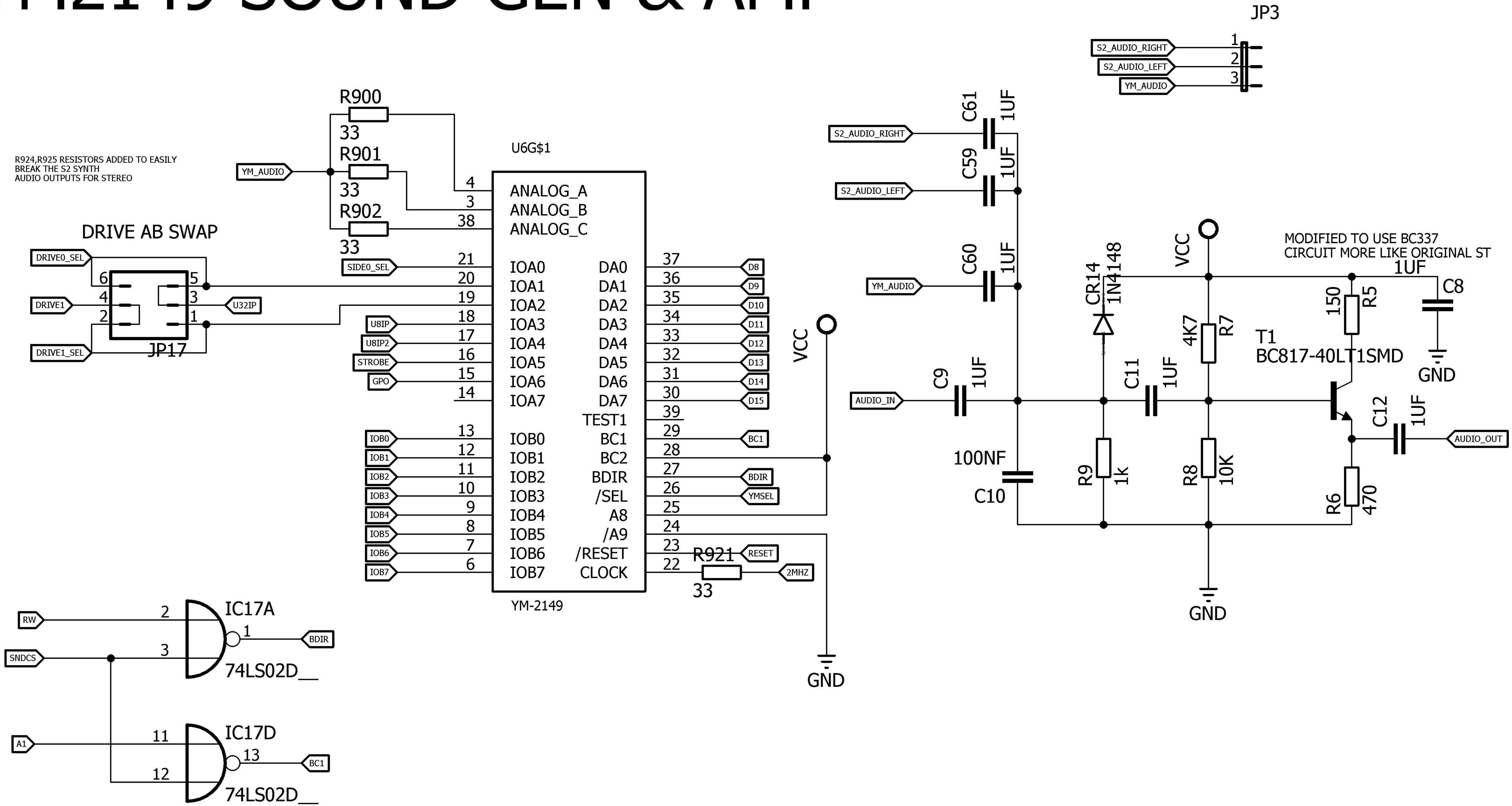
FMCII RTC


G1
VCC
1
X1
VCC1
16
2
X2
VCC0
15
3
A2
/WE
BAT2
14
4
BVCC
BAT1
/RST
13
5
GND
/OE
12
LDS
6
A1
D
/CEI
11
ROM3
7
D0
Q
/CEO
10
ROM3_CART
8
GND1
ROM_/RAM
9
BATTERY
BVCC
0V
0V
GND
GND
GND

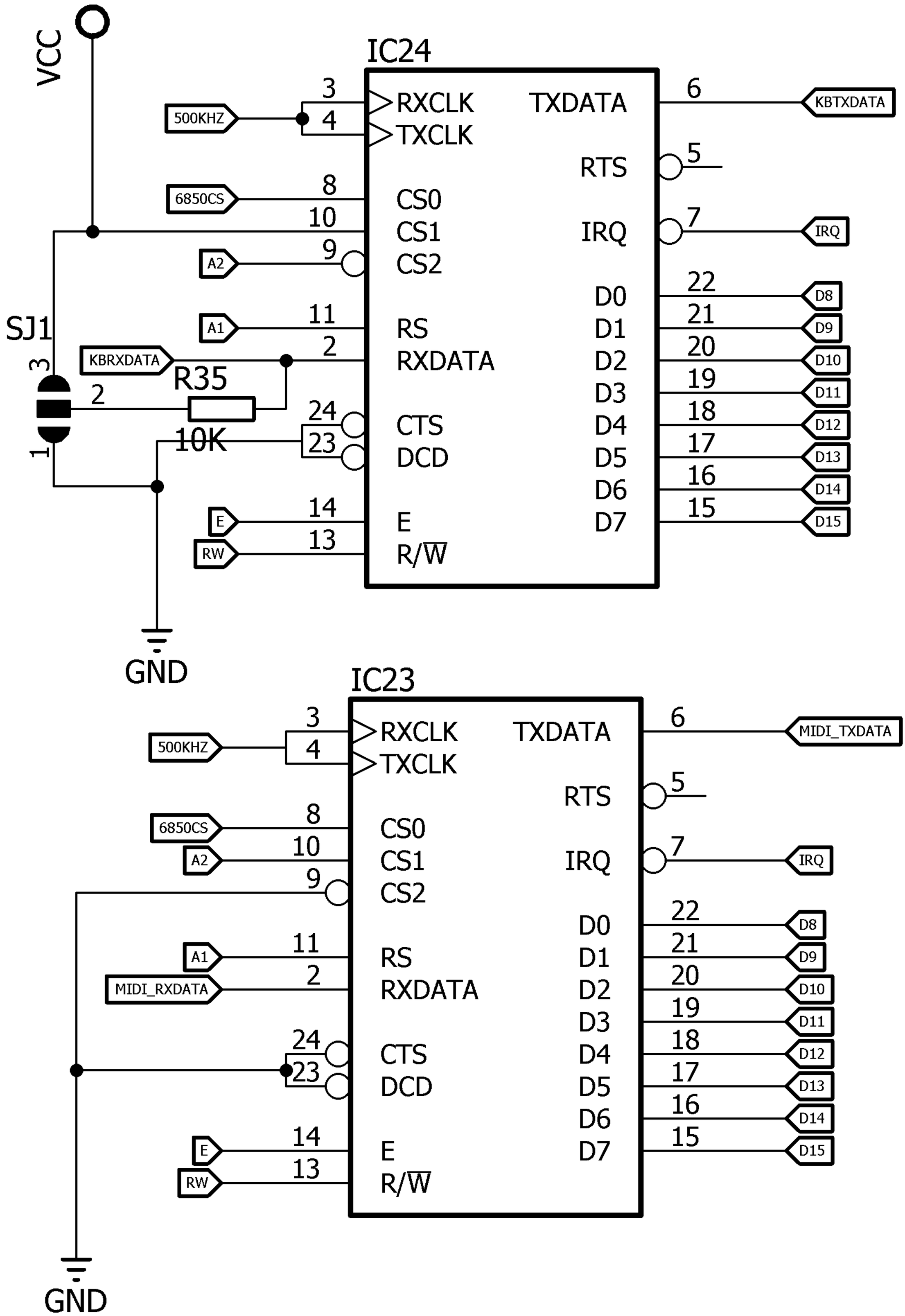
YM2149 SOUND GEN & AMP

R900,R901,R902 RESISTORS ADDED TO EASILY BREAK THE AUDIO OUTPUTS FOR STEREO OR 3 AUDIO CHANS ETC

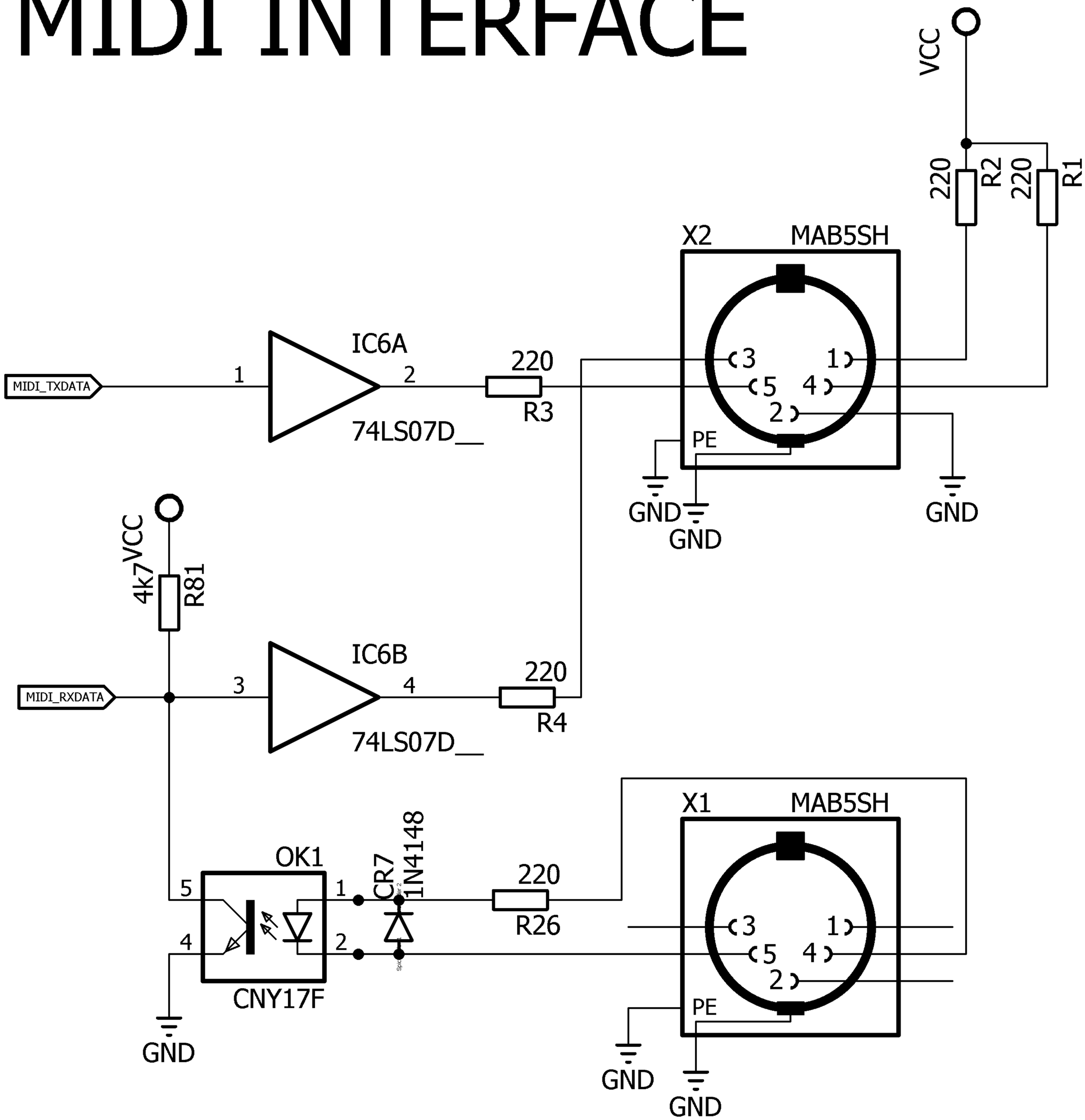
R924,R925 RESISTORS ADDED TO EASILY BREAK THE S2 SYNTH AUDIO OUTPUTS FOR STEREO



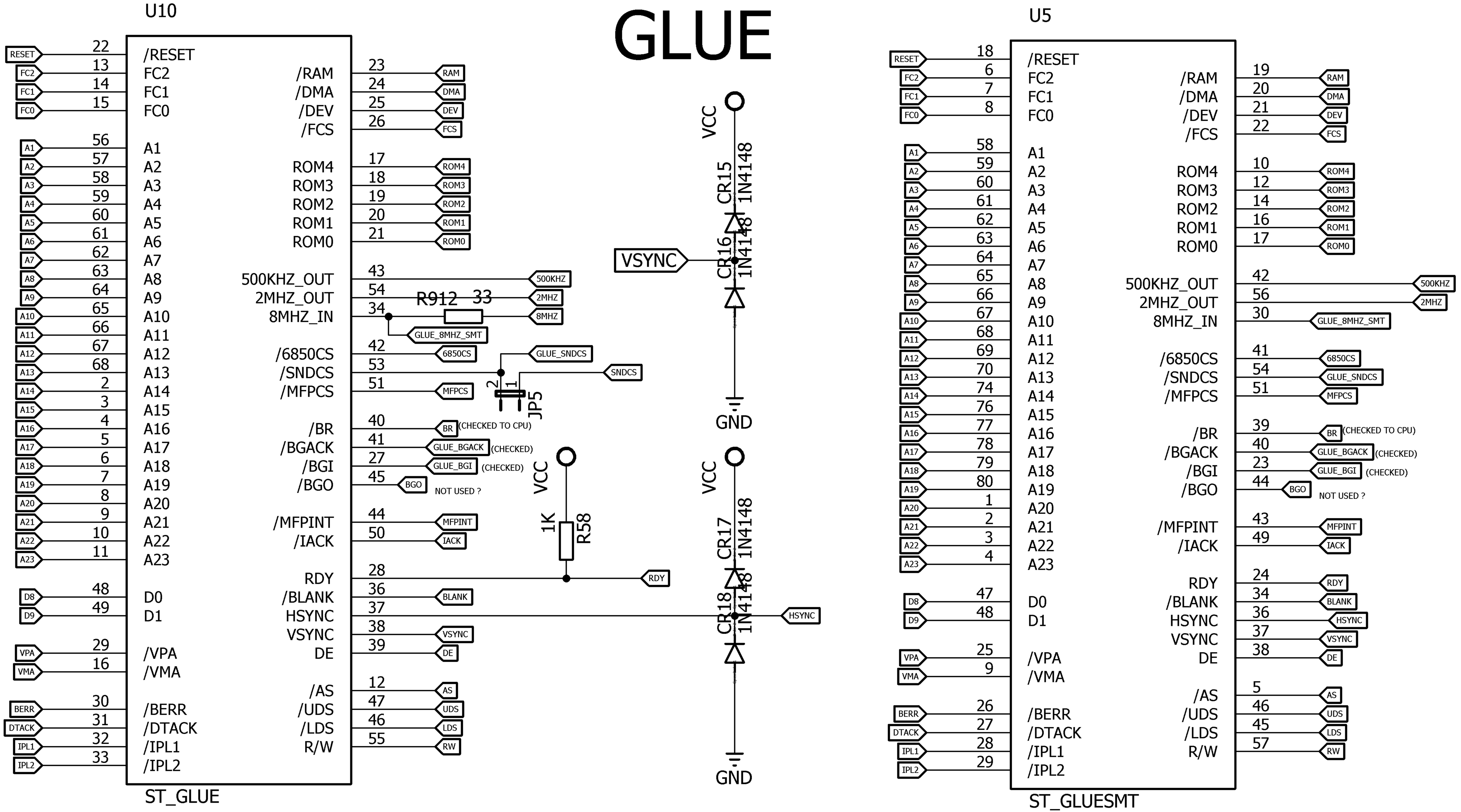
ACIA


VCC
IC24
3
4
500KHZ
RXCLK
TXCLK
TXDATA
6
KBTXDATA
RTS
5
8
6850CS
CS0
10
CS1
IRQ
7
IRQ
9
A2
CS2
D0
22
D8
D1
21
D9
11
A1
RS
SJ1
2
KBRXDATA
RXDATA
D2
20
D10
3
R35
D3
19
D11
2
24
CTS
D4
18
D12
1
10K
23
DCD
D5
17
D13
D6
16
D14
14
E
E
D7
15
D15
13
RW
R/W
GND
IC23
3
4
500KHZ
RXCLK
TXCLK
TXDATA
6
MIDI_TXDATA
RTS
5
8
6850CS
CS0
10
A2
CS1
IRQ
7
IRQ
9
CS2
D0
22
D8
11
A1
RS
D1
21
D9
2
MIDI_RXDATA
RXDATA
D2
20
D10
D3
19
D11
24
CTS
D4
18
D12
23
DCD
D5
17
D13
D6
16
D14
14
E
E
D7
15
D15
13
RW
R/W
GND

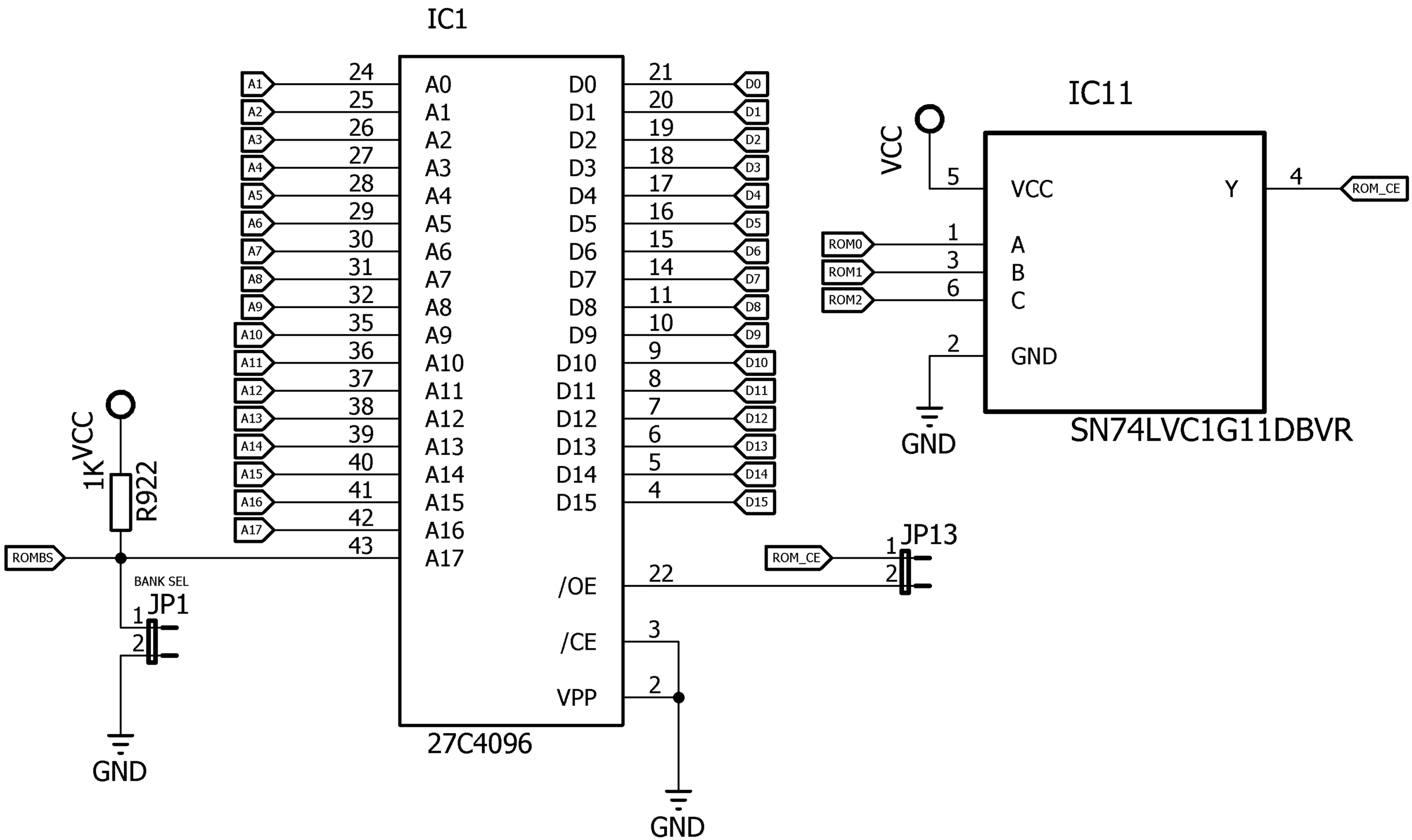
MIDI INTERFACE



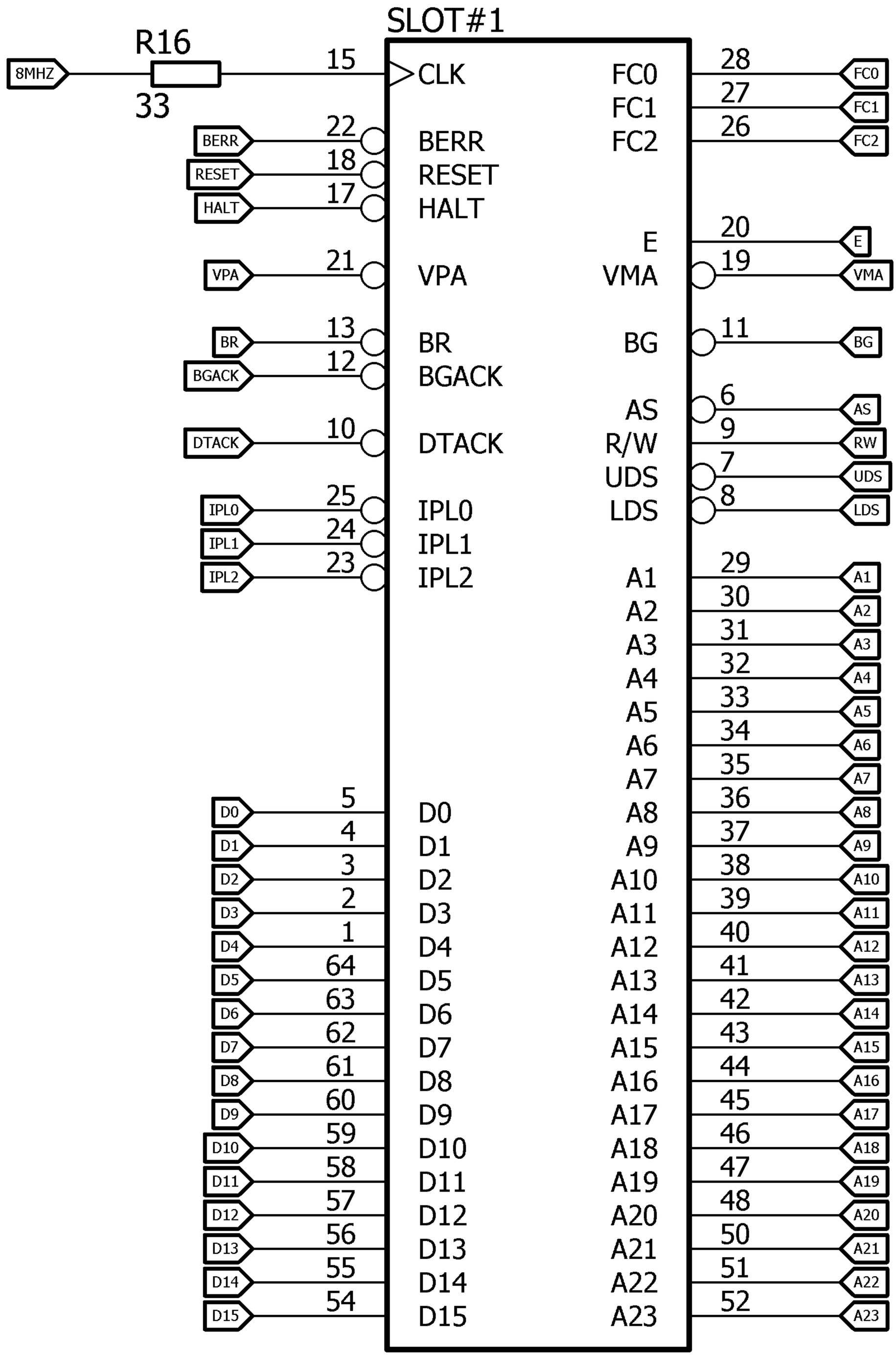
GLUE


U10
ST_GLUE
/RESET
FC2
FC1
FC0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
A23
D0
D1
/VPA
/VMA
/BERR
/DTACK
/IPL1
/IPL2
/RAM
/DMA
/DEV
/FCS
ROM4
ROM3
ROM2
ROM1
ROM0
500KHZ_OUT
2MHZ_OUT
8MHZ_IN
/6850CS
/SNDCS
/MFPCS
/BR
/BGACK
/BGI
/BGO
/MFPINT
/IACK
RDY
/BLANK
HSYNC
VSYNC
DE
/AS
/UDS
/LDS
R/W
R912 33
GLUE_8MHZ_SMT
GLUE_SNDCS
JP5
(CHECKED TO CPU)
(CHECKED)
NOT USED ?
VCC
1K
R58
CR15
CR16
CR17
CR18
1N4148
GND
U5
ST_GLUESMT

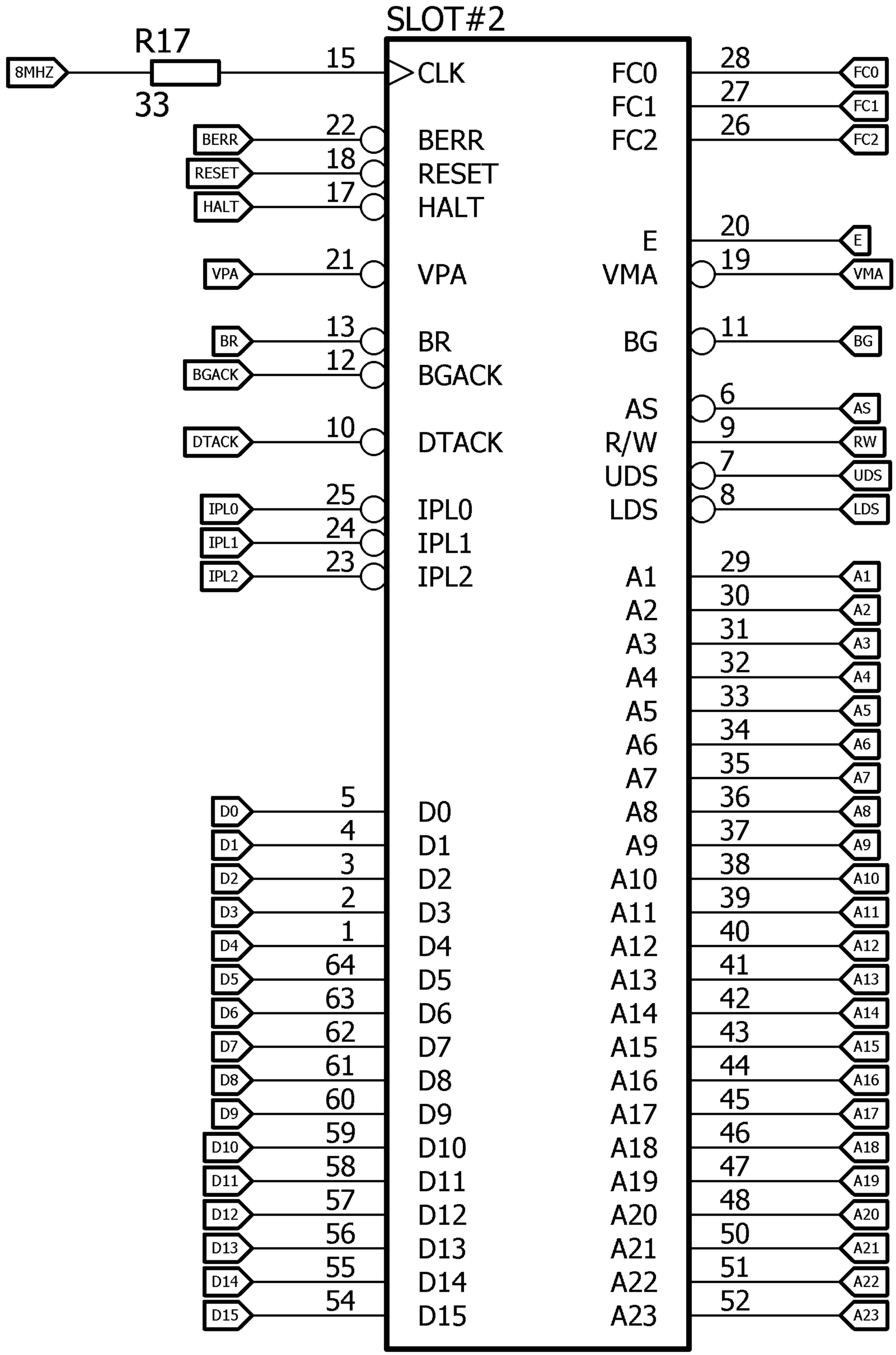
ROM


IC1
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
/OE
/CE
VPP
27C4096
IC11
VCC
Y
A
B
C
GND
SN74LVC1G11DBVR
ROM0
ROM1
ROM2
ROM_CE
JP13
JP1
BANK SEL
ROMBS
R922
1K
VCC
GND

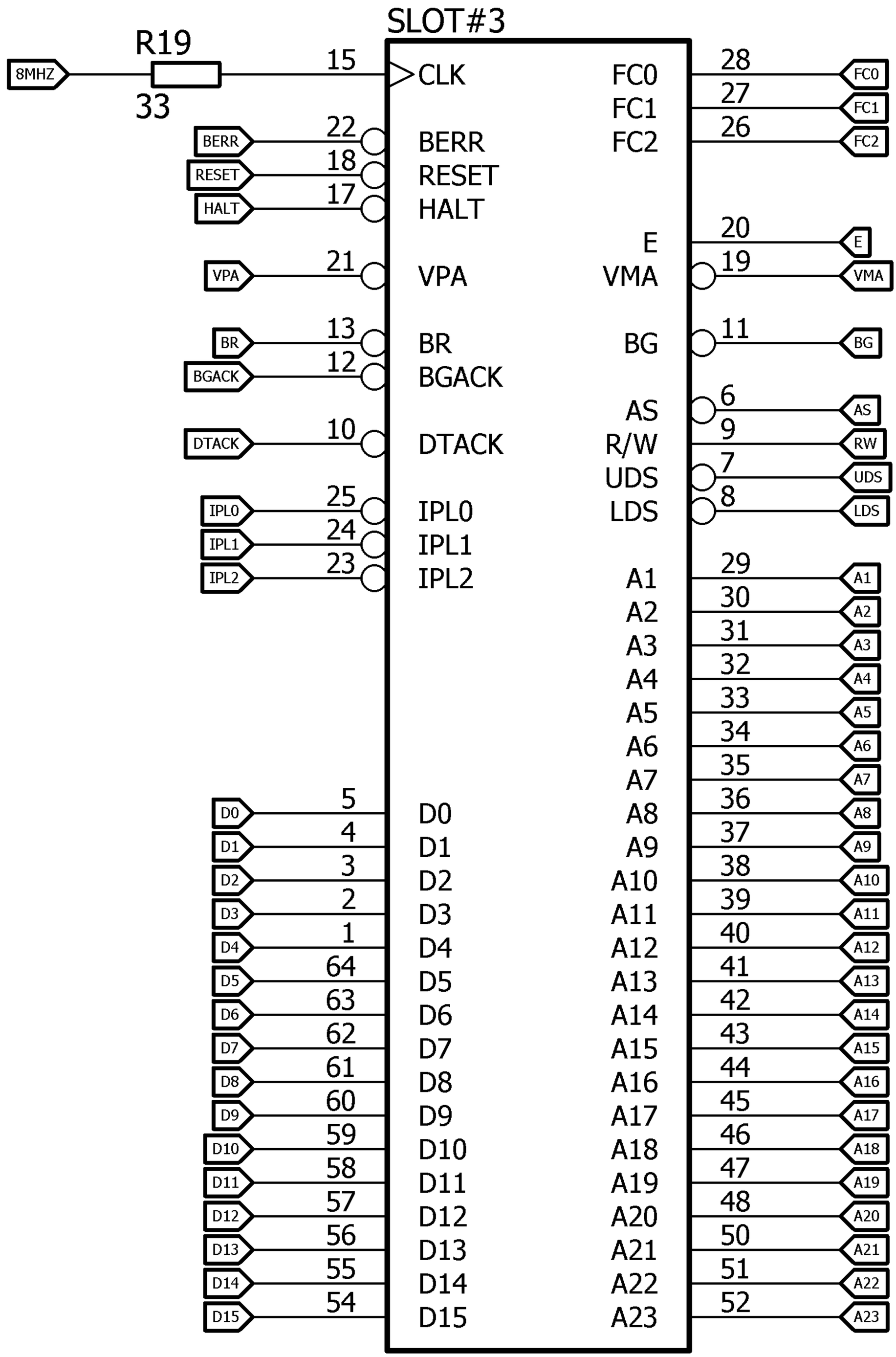
68000 EXPANSION



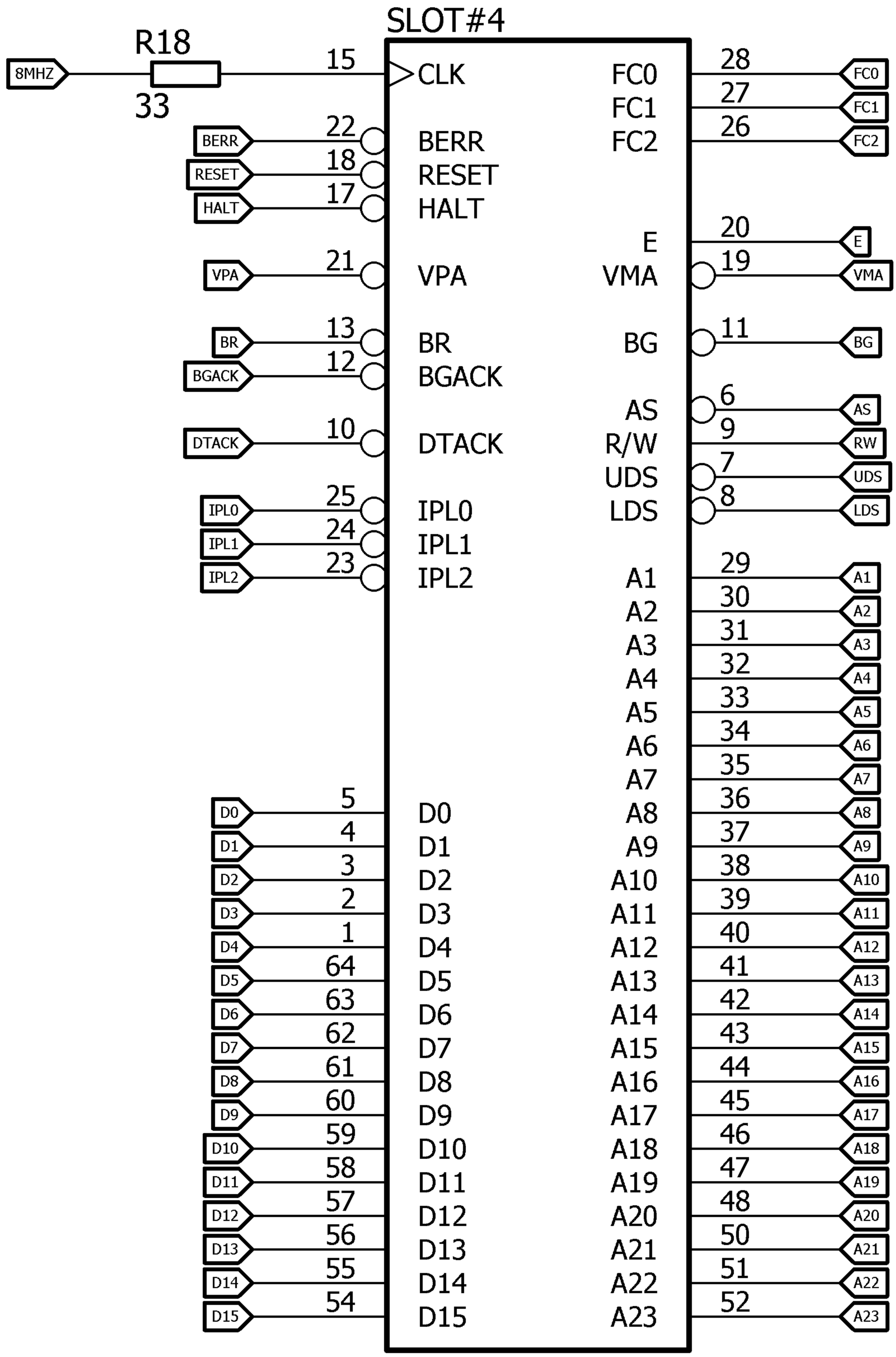
68000 EXPANSION



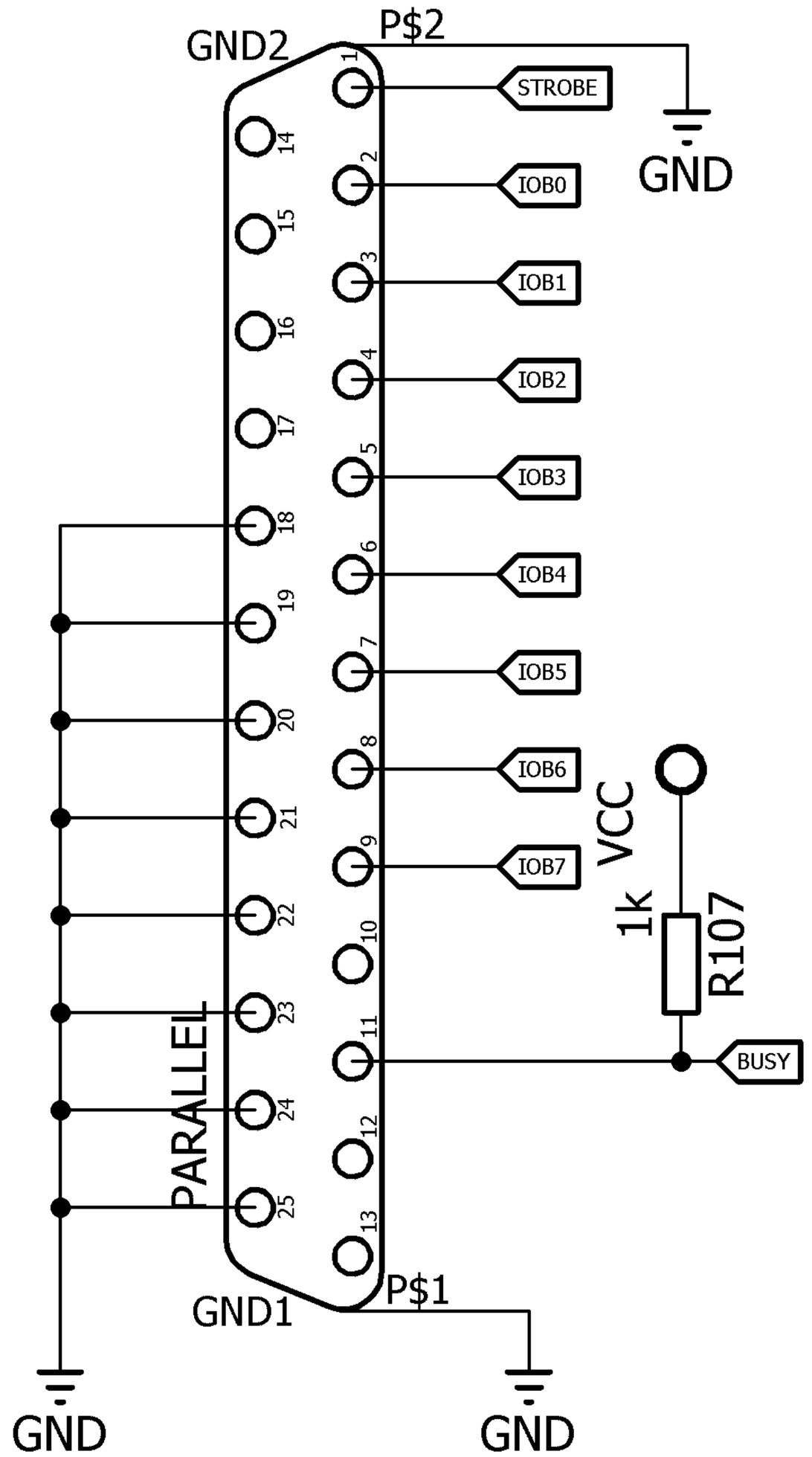
68000 EXPANSION



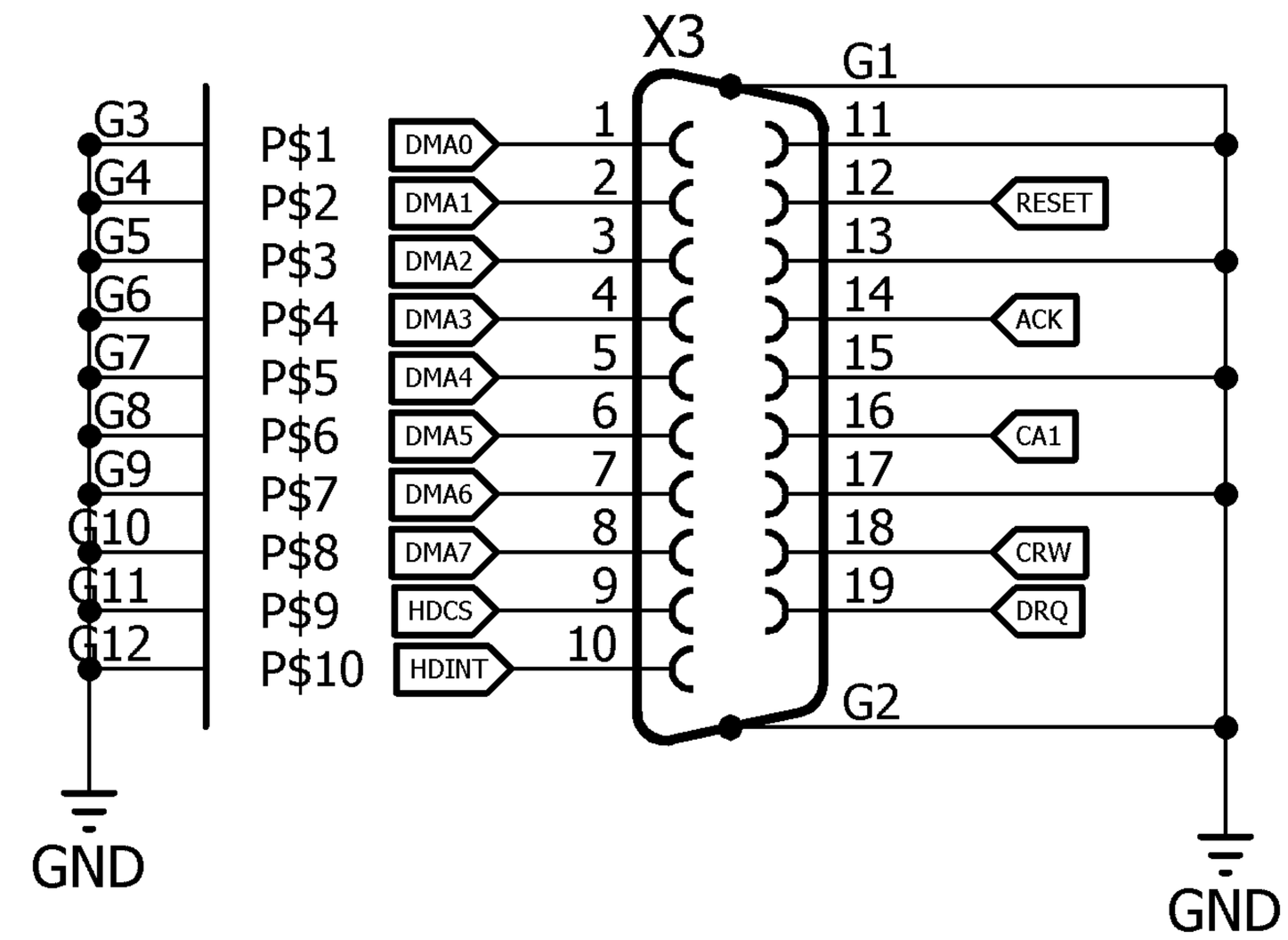
68000 EXPANSION

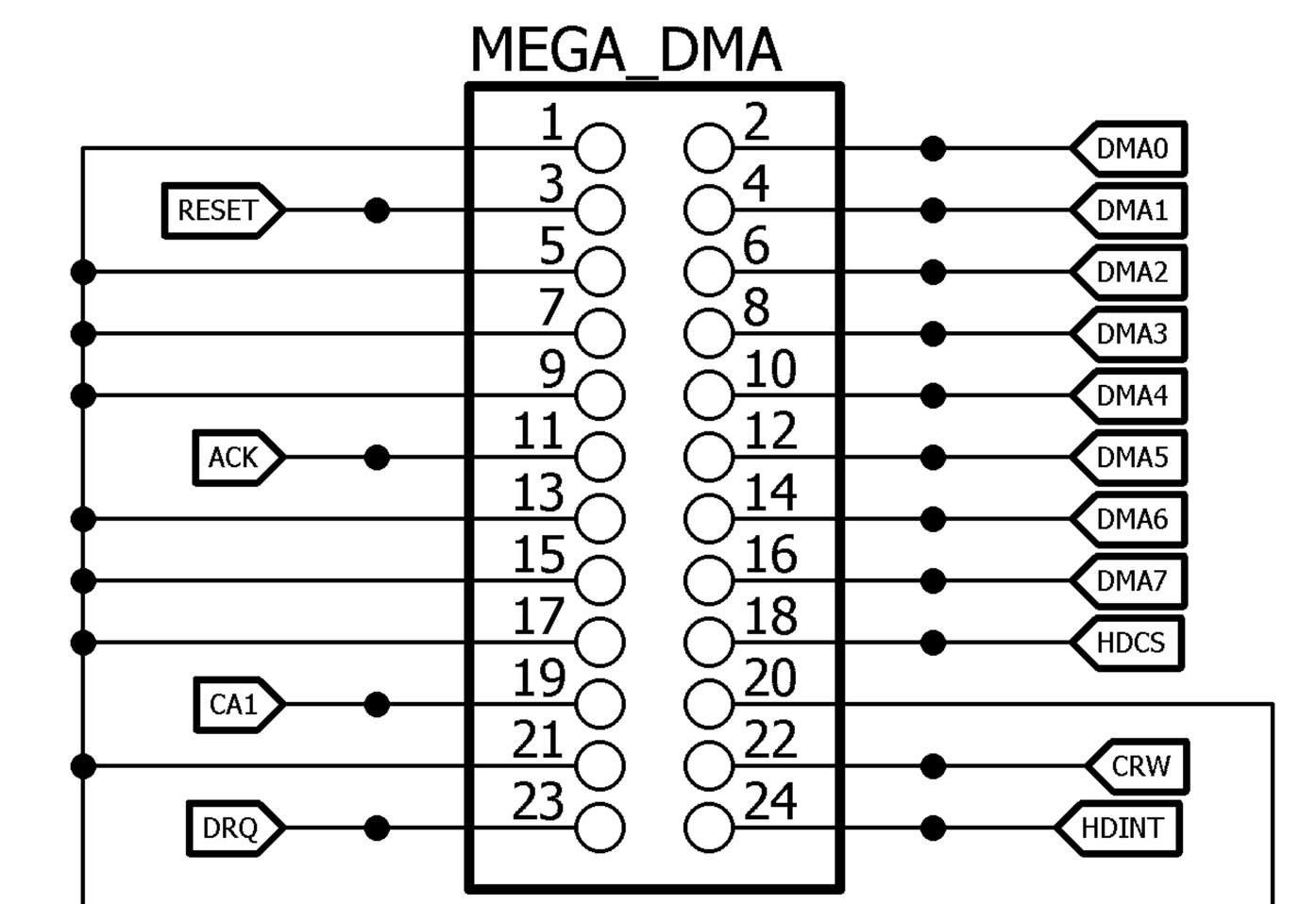


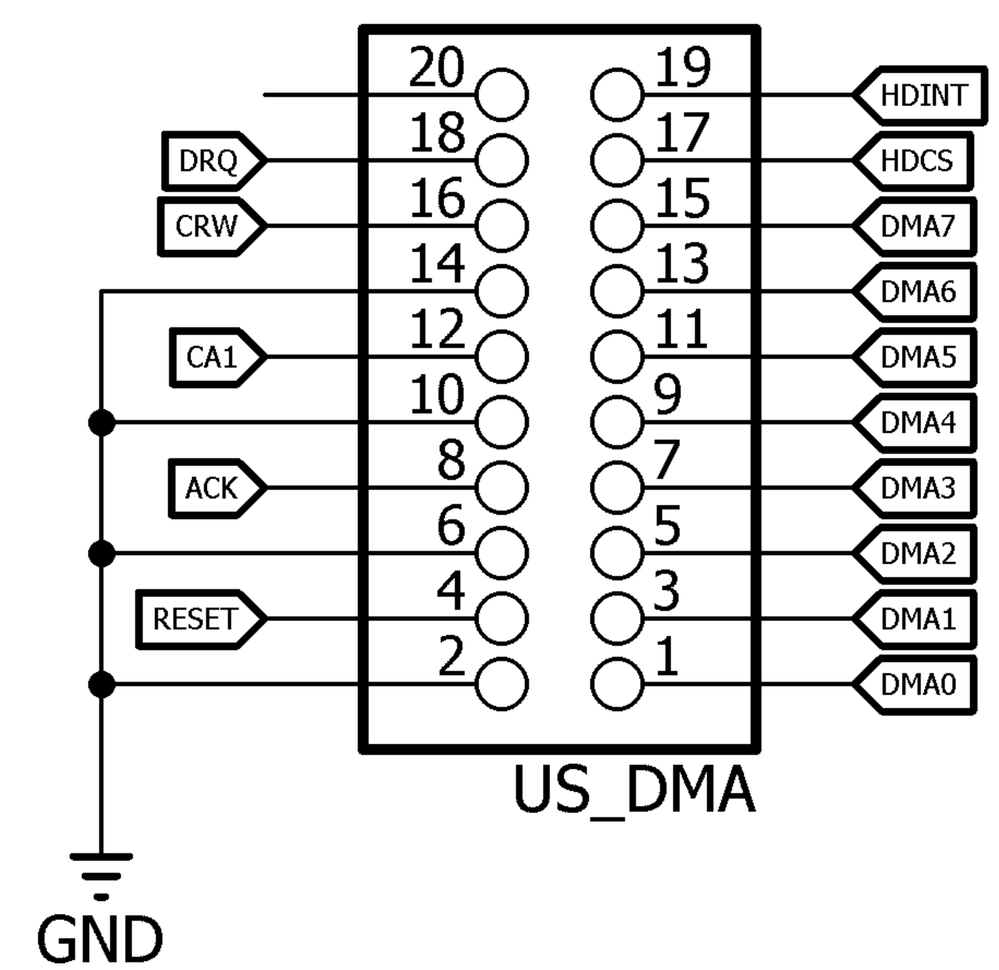
IO CONNECTORS



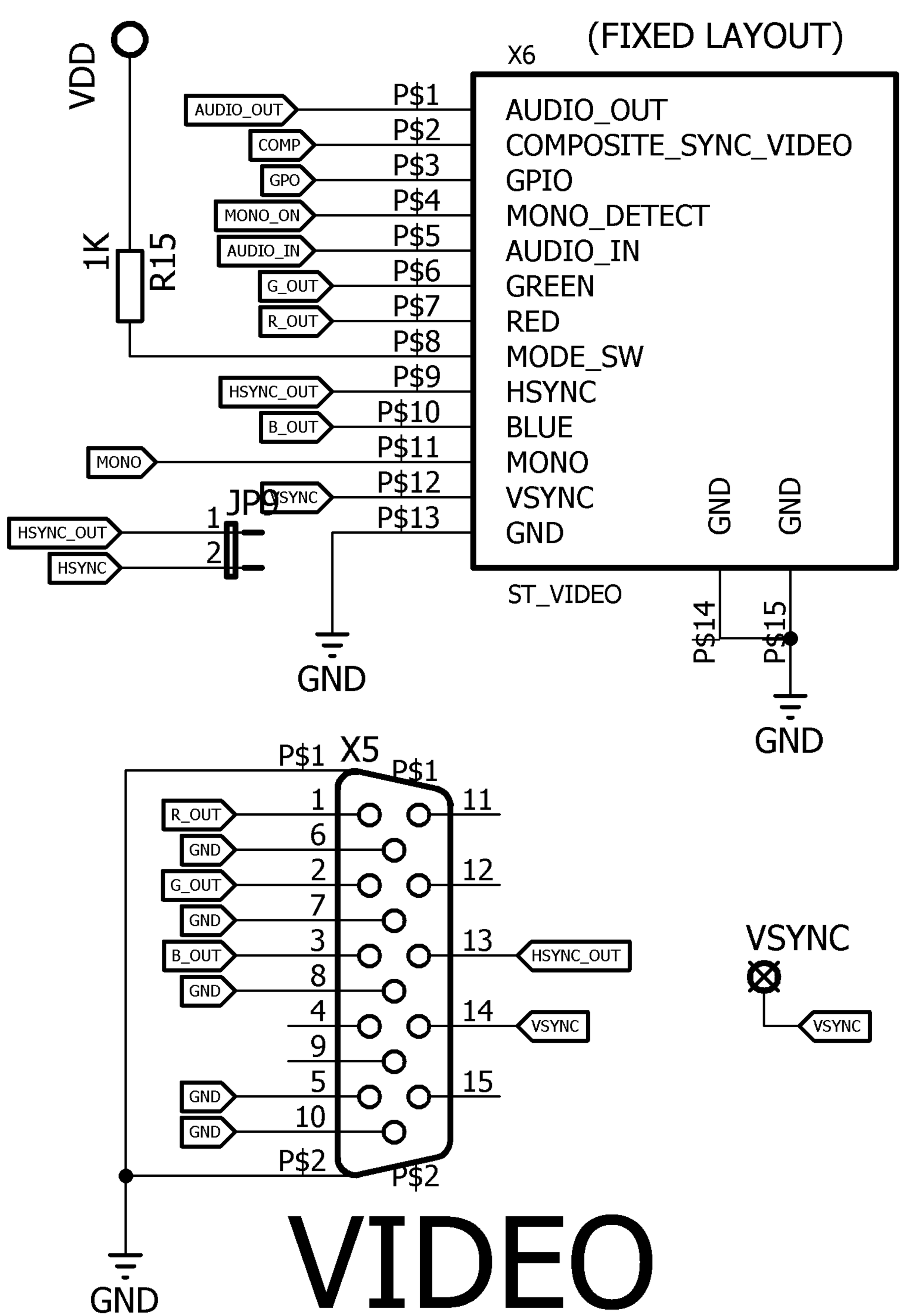
PARALLEL

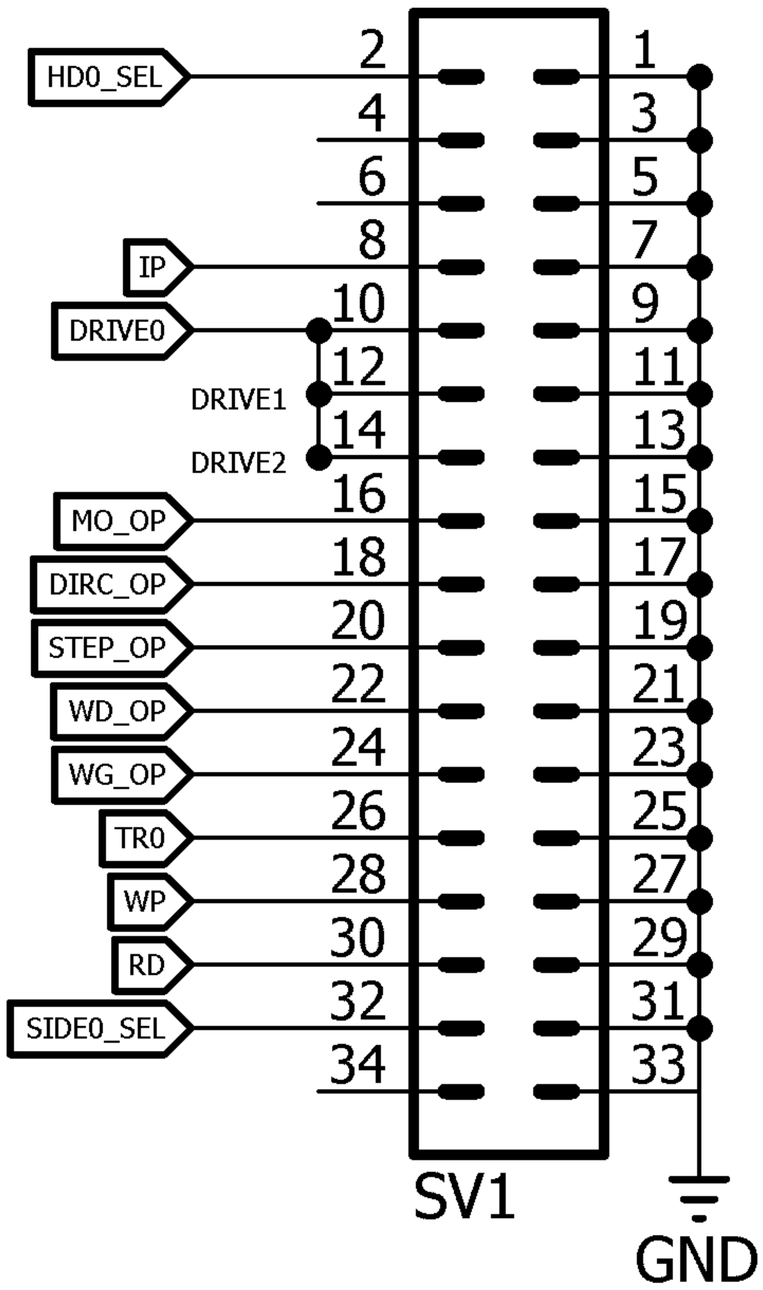




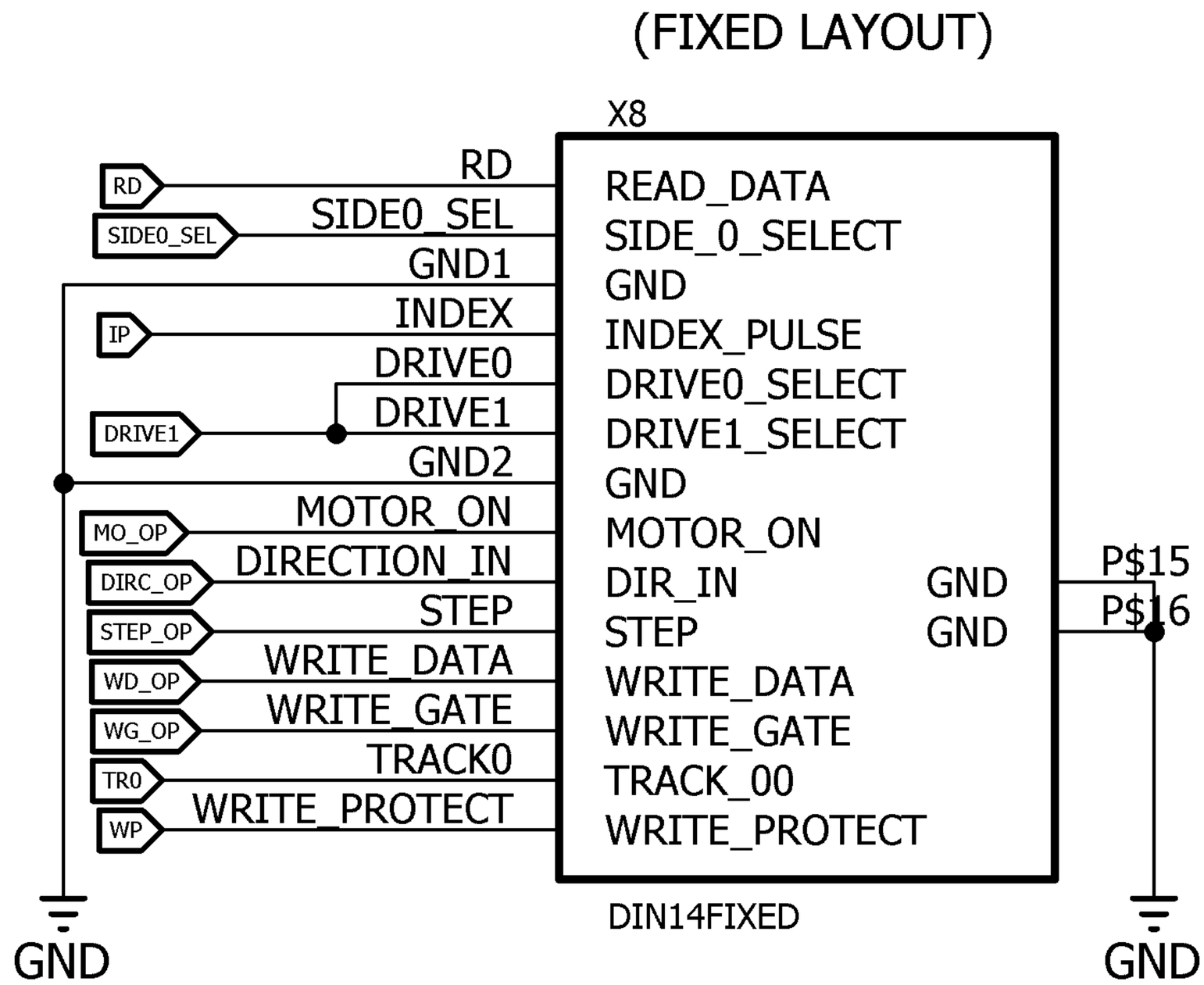


DMA

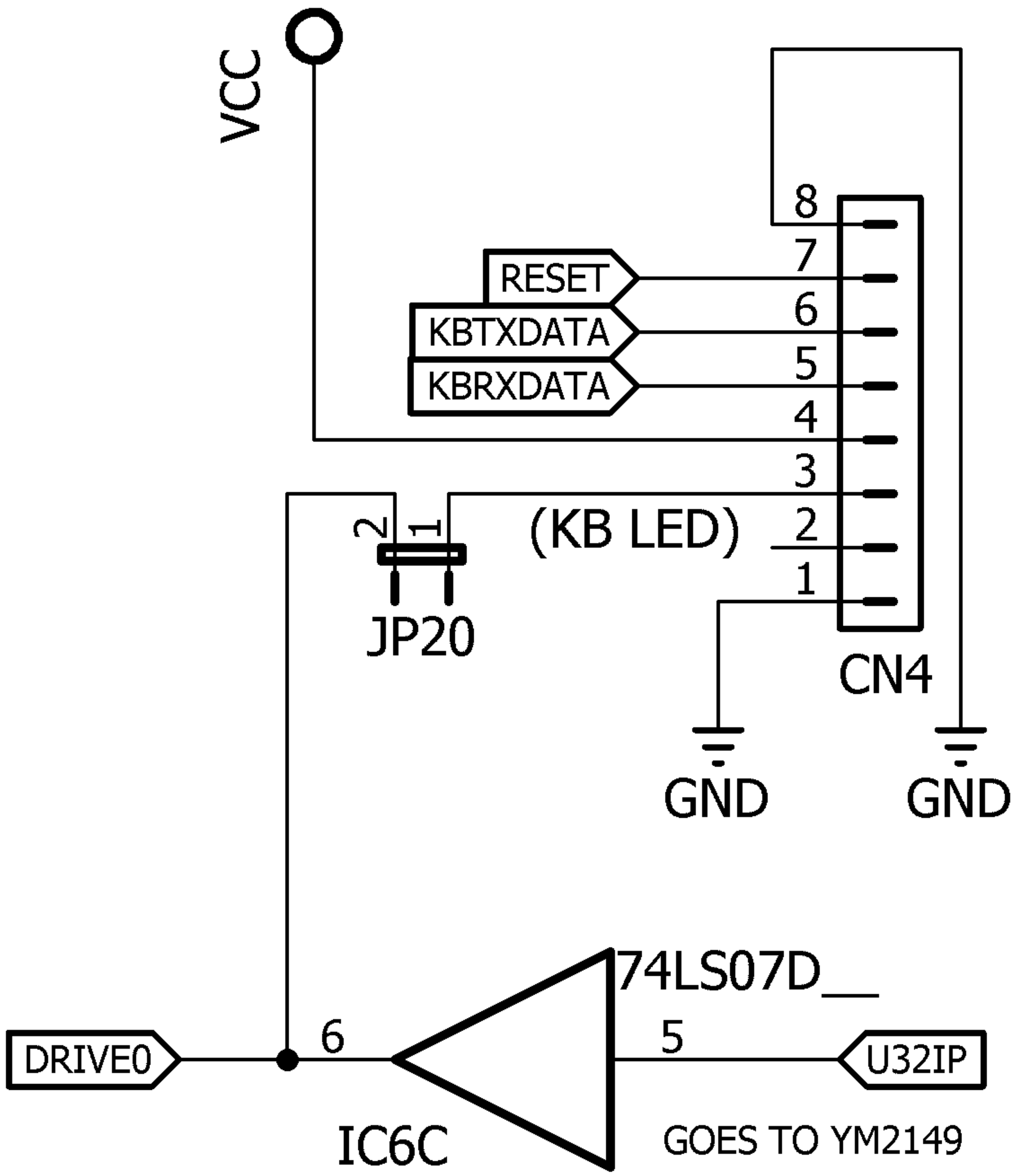

(FIXED LAYOUT)
X6
VDD
1K
R15
AUDIO_OUT
COMP
GPO
MONO_ON
AUDIO_IN
G_OUT
R_OUT
HSYNC_OUT
B_OUT
MONO
VSYNC
HSYNC_OUT
HSYNC
JP9
P$1
P$2
P$3
P$4
P$5
P$6
P$7
P$8
P$9
P$10
P$11
P$12
P$13
AUDIO_OUT
COMPOSITE_SYNC_VIDEO
GPIO
MONO_DETECT
AUDIO_IN
GREEN
RED
MODE_SW
HSYNC
BLUE
MONO
VSYNC
GND
GND
GND
ST_VIDEO
P$14
P$15
GND
GND
X5
P$1
P$1
R_OUT
GND
G_OUT
GND
B_OUT
GND
GND
GND
HSYNC_OUT
VSYNC
VSYNC
P$2
P$2
GND
VIDEO



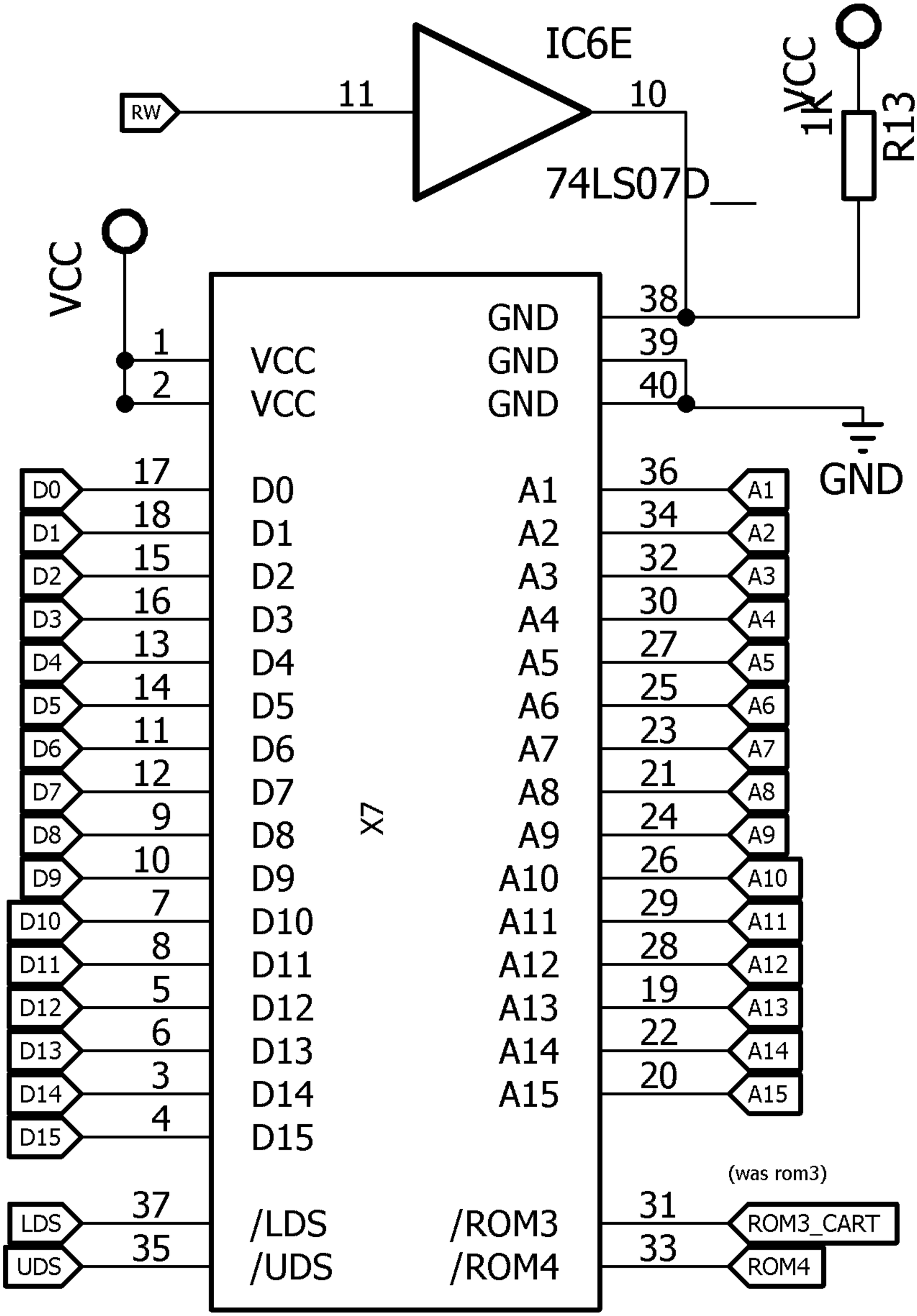
FLOPPY INT



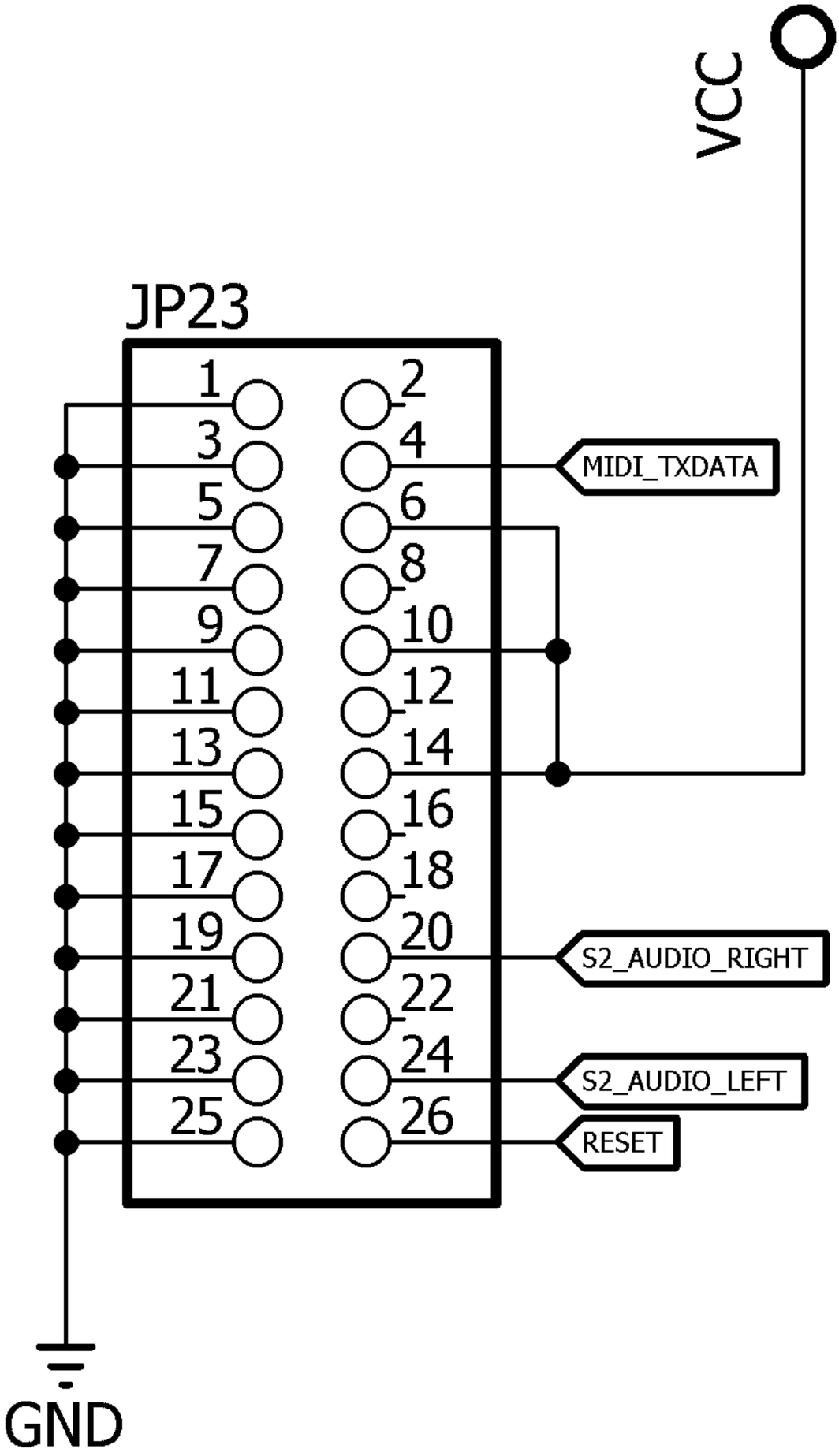
FLOPPY EXT


VCC
RESET
KBTXDATA
KBRXDATA
8
7
6
5
4
3
2
1
(KB LED)
2
1
JP20
CN4
GND
GND
74LS07D__
DRIVE0
6
5
U32IP
IC6C
GOES TO YM2149

KEYBOARD

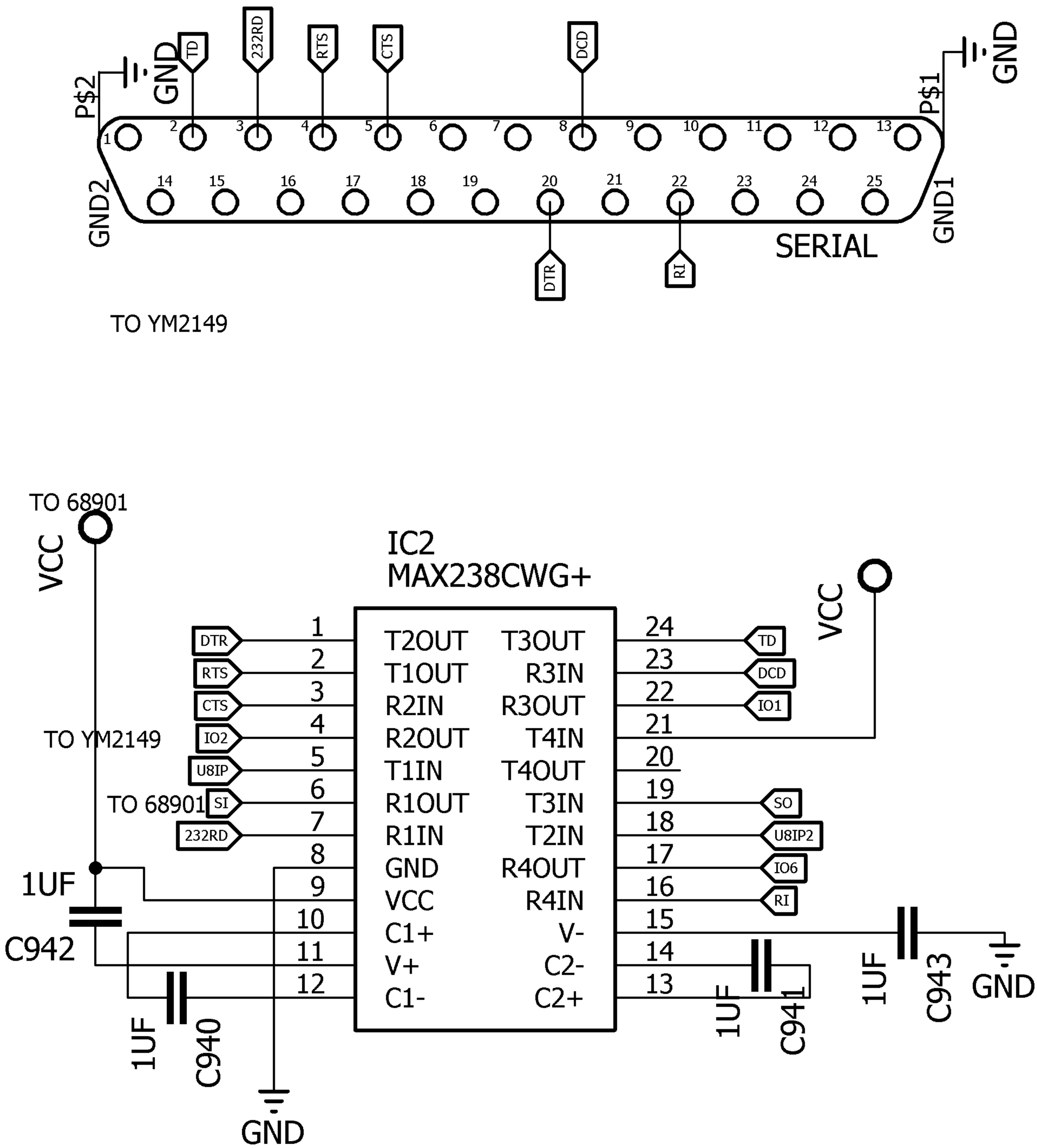

IC6E
74LS07D__
RW
11
10
VCC
1K
R13
VCC
1
2
VCC
VCC
GND
GND
GND
38
39
40
GND
X7
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
17
18
15
16
13
14
11
12
9
10
7
8
5
6
3
4
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
36
34
32
30
27
25
23
21
24
26
29
28
19
22
20
LDS
UDS
37
35
/LDS
/UDS
/ROM3
/ROM4
(was rom3)
31
33
ROM3_CART
ROM4

CARTRIDGE

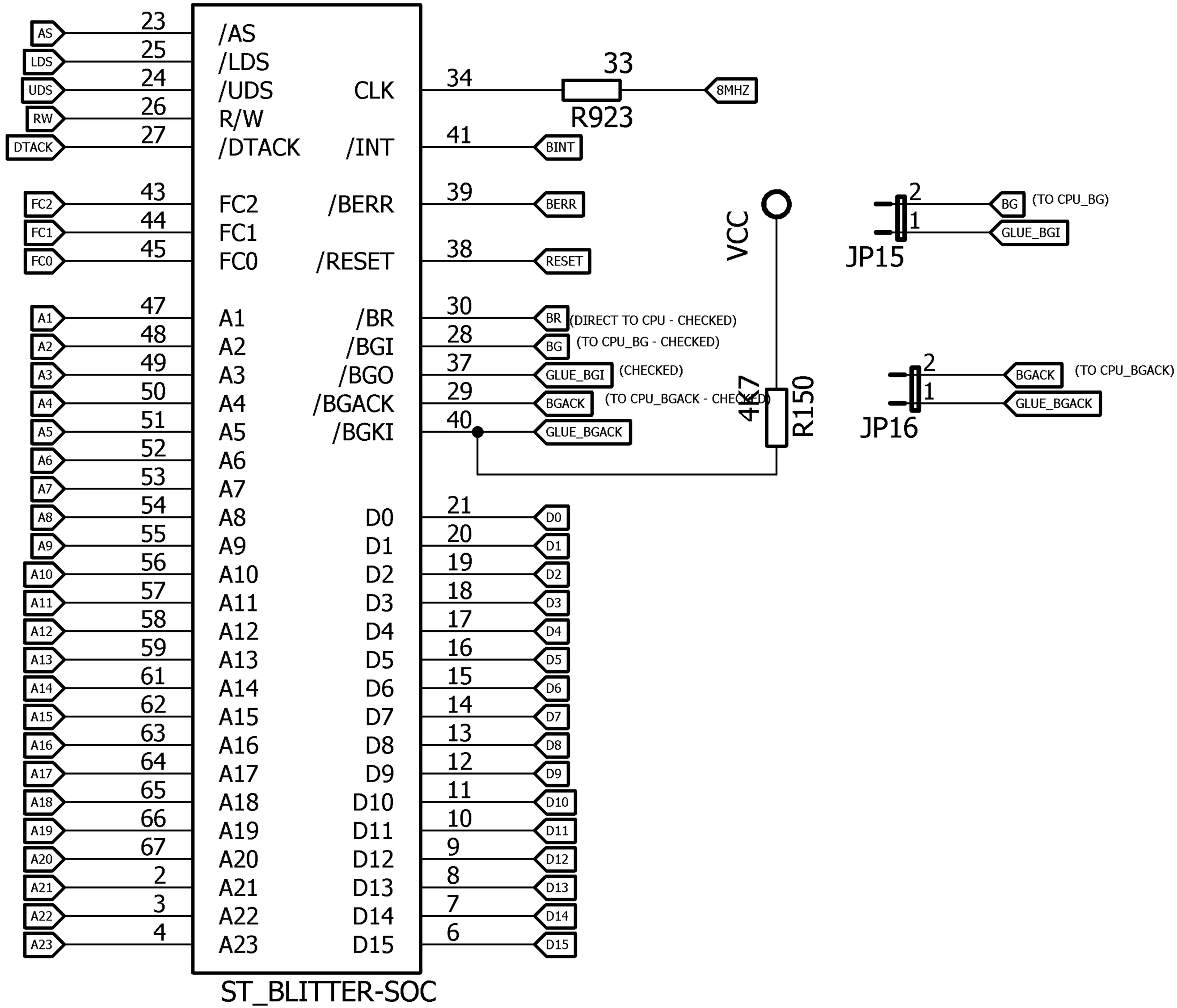


S2 MIDI SYNTH

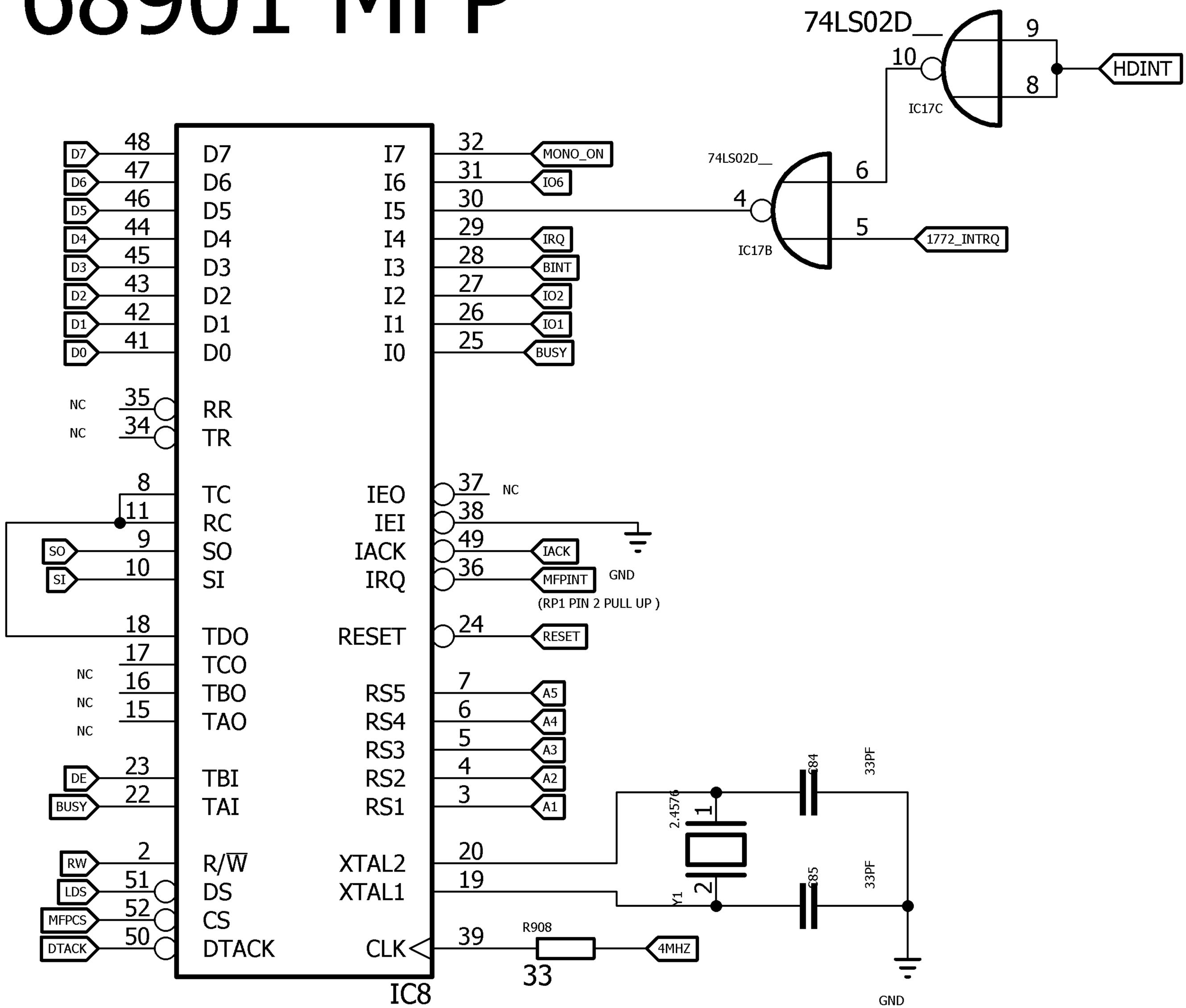
RS232 INTERFACE



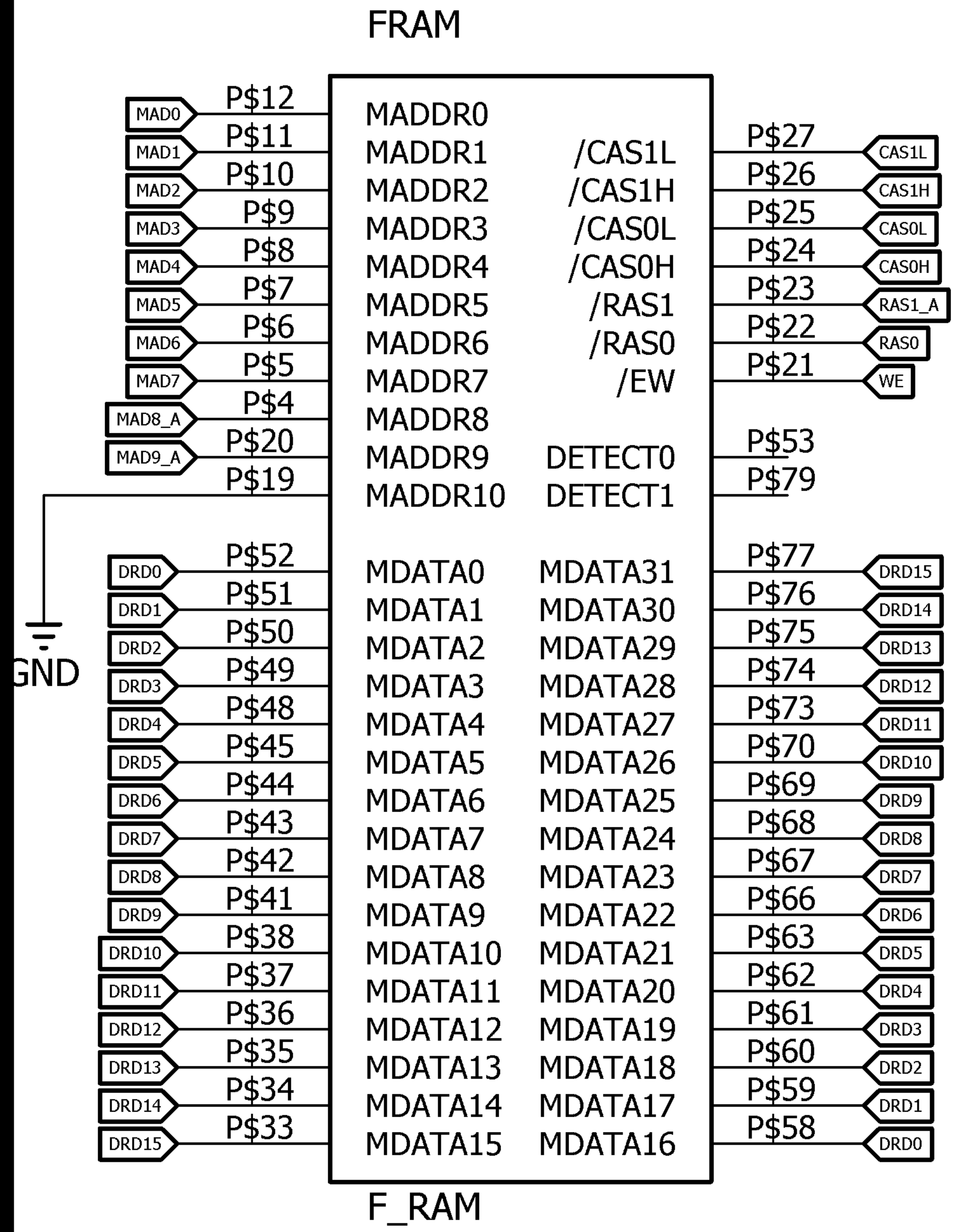
BLITTER


U3
/AS
/LDS
/UDS
R/W
/DTACK
CLK
/INT
FC2
FC1
FC0
/BERR
/RESET
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
A23
/BR
/BGI
/BGO
/BGACK
/BGKI
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
ST_BLITTER-SOC
AS
LDS
UDS
RW
DTACK
FC2
FC1
FC0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
A23
23
25
24
26
27
43
44
45
47
48
49
50
51
52
53
54
55
56
57
58
59
61
62
63
64
65
66
67
2
3
4
34
41
39
38
30
28
37
29
40
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
33
R923
8MHZ
BINT
BERR
RESET
BR
(DIRECT TO CPU - CHECKED)
BG
(TO CPU_BG - CHECKED)
GLUE_BGI
(CHECKED)
BGACK
(TO CPU_BGACK - CHECKED)
GLUE_BGACK
VCC
4K7
R150
JP15
BG
(TO CPU_BG)
GLUE_BGI
JP16
BGACK
(TO CPU_BGACK)
GLUE_BGACK
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15

68901 MFP


74LS02D__
IC17C
74LS02D__
IC17B
HDINT
1772_INTRQ
D7
D6
D5
D4
D3
D2
D1
D0
MONO_ON
IO6
IRQ
BINT
IO2
IO1
BUSY
NC
NC
SO
SI
DE
BUSY
RW
LDS
MFPCS
DTACK
IACK
MFPINT
GND
(RP1 PIN 2 PULL UP)
RESET
A5
A4
A3
A2
A1
4MHZ
R908
33
IC8
2.4576
Y1
684
685
33PF
33PF
GND

DRAM_FALC


FRAM
MADDR0
MADDR1
MADDR2
MADDR3
MADDR4
MADDR5
MADDR6
MADDR7
MADDR8
MADDR9
MADDR10
/CAS1L
/CAS1H
/CAS0L
/CAS0H
/RAS1
/RAS0
/EW
DETECT0
DETECT1
MDATA0
MDATA1
MDATA2
MDATA3
MDATA4
MDATA5
MDATA6
MDATA7
MDATA8
MDATA9
MDATA10
MDATA11
MDATA12
MDATA13
MDATA14
MDATA15
MDATA31
MDATA30
MDATA29
MDATA28
MDATA27
MDATA26
MDATA25
MDATA24
MDATA23
MDATA22
MDATA21
MDATA20
MDATA19
MDATA18
MDATA17
MDATA16
MAD0 P$12
MAD1 P$11
MAD2 P$10
MAD3 P$9
MAD4 P$8
MAD5 P$7
MAD6 P$6
MAD7 P$5
MAD8_A P$4
MAD9_A P$20
P$19
GND
DRD0 P$52
DRD1 P$51
DRD2 P$50
DRD3 P$49
DRD4 P$48
DRD5 P$45
DRD6 P$44
DRD7 P$43
DRD8 P$42
DRD9 P$41
DRD10 P$38
DRD11 P$37
DRD12 P$36
DRD13 P$35
DRD14 P$34
DRD15 P$33
P$27 CAS1L
P$26 CAS1H
P$25 CAS0L
P$24 CAS0H
P$23 RAS1_A
P$22 RAS0
P$21 WE
P$53
P$79
P$77 DRD15
P$76 DRD14
P$75 DRD13
P$74 DRD12
P$73 DRD11
P$70 DRD10
P$69 DRD9
P$68 DRD8
P$67 DRD7
P$66 DRD6
P$63 DRD5
P$62 DRD4
P$61 DRD3
P$60 DRD2
P$59 DRD1
P$58 DRD0
F_RAM